

Design of Silicon-based Equalization Techniques

For Band-limited Giga-Hertz Channels

A Dissertation
Presented to
The Academic Faculty

by

Hyoung Soo Kim

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2010

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Design of Silicon-based Equalization Techniques

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Approved by:

Dr. Joy Laskar, Advisor
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Emmanouil Tentzeris,
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Saibal Mukhopadhyay,
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Gee-kung Chang,
School of Electrical and Computer
Engineering
Georgia Institute of Technology

Dr. Steven Danyluk,
School of Mechanical Engineering
Georgia Institute of Technology

Date Approved: December, 14, 2010

ACKNOWLEDGEMENTS

It has been a great experience to study at Georgia Institute of Technology. It has been an exciting journey with a lot of collaborations with industrial companies and fellow students and researchers. I think this experience will benefit rest of my life.

First, I would like to acknowledge my advisor, Professor Joy Laskar for his guidance and support. He gives us an inspiration and shows us a passion for his research work. I also would like to thank you my committee members, Professor Emmanouil Tentzeris, Professor Gee-kung Chang, Professor Steven Danyluk and Professor Saibal Mukhopadhyay for their advice and time.

I also am indebted to Dr. Edward Gebara for leading our mixed-signal research group. He gave me the opportunity to be a part of his team and grow as an electrical engineer. I am grateful to have my past and present co-researchers, Dr. Moonkyun Maeng, Dr. Youngsik Hur, Dr. Franklin Bien, Dr. Soumya Chandramouli, Dr. Carl Chun, Dr. Chris Scholtz, Jean de Ginestous. Debesh Bhatta, and Kil-hoon Lee.

I would like to thank you Dr. Chang-ho Lee and Dr. Kyutae Lim for their support and guidance during my Ph. D years. Old K-MAG members, who are in Korea, always make me feel at home, Dr. Sangwoo Han, Dr. Seungyup Woo, Dr. Sangwoong Yoon, and Dr. Jinsung Park.

My coffee-break members, Sanghyun Woo, David Chung, Joonhoi Hur and Dr. Jonghoon Lee, are always there to discuss any kinds of matters.

I have spent two great summers in Cambridge, working at Lyric Semiconductor and want to thank you Dr. Ben Vigoda, David Reynolds and Alex Alexeyev.

Finally I would like to thank you my parents. Especially they help me go through two knee reconstruction surgeries during my Georgia Tech years when I hurt myself playing basketball. They spent quite a time in Atlanta to look after me and my sister. I would not accomplish my work without their help.

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LIST OF SYMBOLS AND ABBREVIATIONS

BER	Bit-Error Rate
BERT	Bit-Error Rate Test
BPF	Band Pass Filter
CD	Chromatic Dispersion
CMOS	Complimentary Metal Oxide Semiconductor
CP	Charge Pump
CW	Continuous Wave
DAC	Digital-to-Analog Converter
DFE	Decision-Feedback Equalizer
DLL	Delay-Locked Loop
DMD	Differential Modal Dispersion
FFE	Feed-Forward Equalizer
FIR	Finite-Impulse Response
FSE	Fractionally Spaced Equalizer
GPON	Giga-bit Passive Optical Network
IC	Integrated Circuit
ISI	Inter-Symbol Interference
LE	Linear Equalizer
LMS	Least Mean Square
LMSE	Least-Mean Square Error
LPF	Low Pass Filter
MLSD	Maximum Likelihood Sequence Detection
MMF	Multi-Mode Fiber
MMSE	Minimum Mean Square Error
NEXT	Near End Cross Talk
NMOS	N-type Metal Oxide Semiconductor
NRZ	None Return-to-Zero
PAM	Pulse Amplitude Modulation
PD	Phase Detector
PMD	Polarization Mode Dispersion
PMOS	P-type Metal Oxide Semiconductor
PRBS	Pseudo Random Bit Sequence
PRML	Partial Response Maximum Likelihood
SMF	Single Mode Fiber
TD-OM	Transition Detector-based Output Monitoring
VGA	Variable Gain Amplifier
VTGA	Variable Tap-Gain Amplifier
ZF	Zero Forcing

SUMMARY

The object of this research is to develop a solution for band-limited channels. Backplane channels and GPON channels are investigated to apply an equalization technique. Different lengths of backplane channels are measured with different signal speeds to investigate the channel performance. Also a GPON system with different fiber lengths is designed and set up in a lab to measure the BER performance. The GPON system utilizes a Fabry-Perot laser for the most economical solution. After the circuits are fabricated, they are inserted into the system to measure the performance of the channels with equalizers. Both the backplane and the GPON system show successful channel improvement in measured eye diagrams and BER. To expedite the procedure and eventually build an adaptive system which could be inserted and self-optimizing, we found it essential to monitor the output of the equalizer. A novel analog way to achieve this goal is suggested. All the equalizers mentioned in this dissertation have one summing node to add up all the values from VGAs. This structure is very efficient, but in the event that there are too many VGAs, it draws too much current through the one node. This issue is dealt with by the design of two nine tap equalizers, which are compared to assess the difference in performance between the unbalanced structure and the balanced structure.

CHAPTER I.

INTRODUCTION

Today's technology applications push the limit of available bandwidth, and the increasing use of the Internet and corporate Intranet is fueling the drive to develop solutions for multi-gigabit data transmission through bandwidth limited channels. This demand for high-speed data communication is increasing rapidly. Applications for this high speed link include transferring voice, data and high resolution graphics via coaxial cable, network backplanes, and optical fiber at data rates from 622 Mbps to 10 Gbps with a near

future target of 40 Gbps. The volume of multimedia data has increased tremendously compared to that of traditional voice data. As the data rate increases, the dispersive effect of the channel deteriorates rapidly.

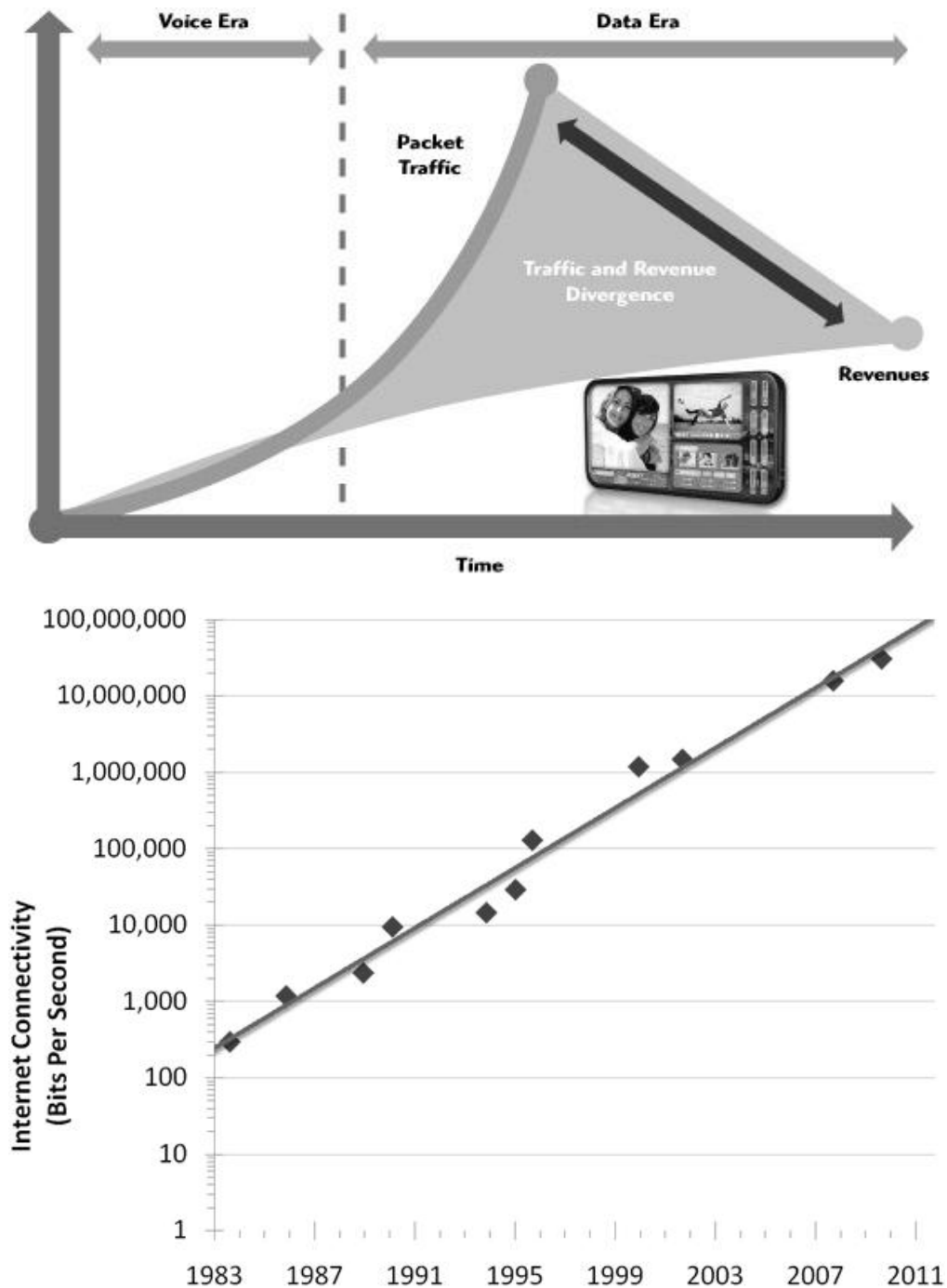


Figure 1-1. Projected increase of data load.

Recently, the communication paradigm has been changing from voice oriented services to image and data oriented services. As shown in Figure 1-1, the load of digital data has surpassed the load of the traditional voice data more than nine times. These changes have resulted from the rapid growth of the Internet and worldwide web and require higher data rates on existing channels.

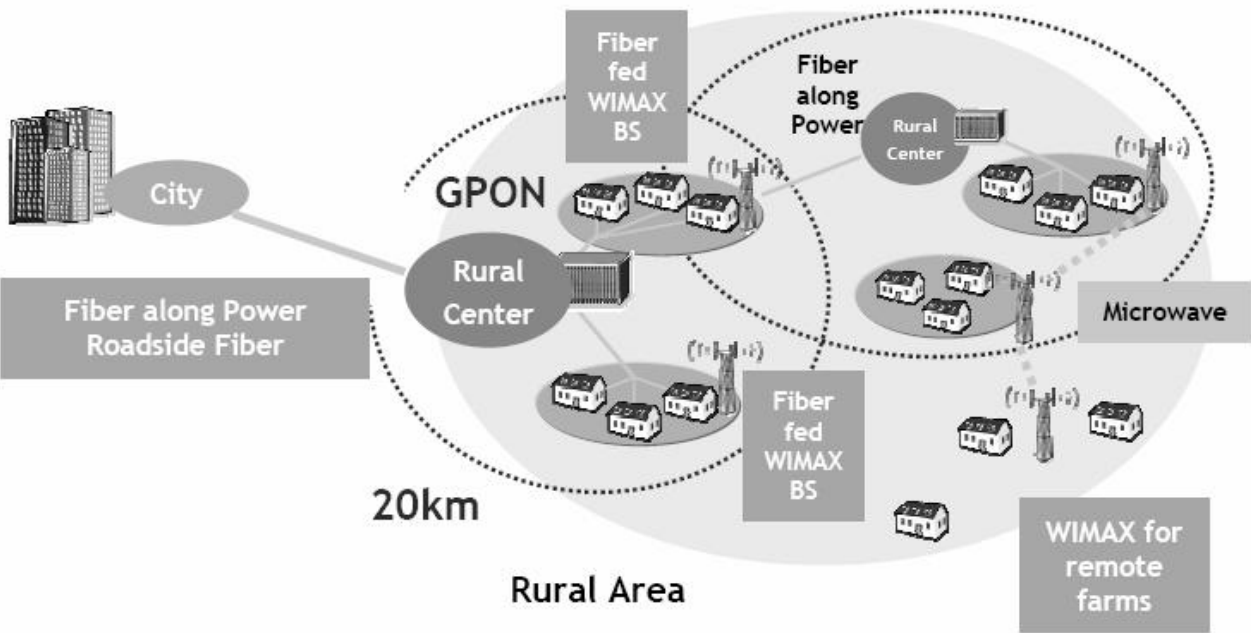


Figure 1-2. Broadband communication system utilizing optical and wireless communication systems.



a)



b)

Figure 1-3. a) Streaming multimedia content over the Internet,
b) Streaming multimedia content in a handheld device through the Internet.

Also various communication techniques work together to make an efficient and broad communication network. For example, wireless (WiMax) and fiber optical channels (Giga-bit Passive Optical Network -GPON) are incorporated to extend the covered area and bandwidth together as shown in Figure 1-2. The GPON system is a bi-directional point-to-multipoint network architecture deploying optical access lines between a carrier's central office and customer sites [1]. Because it is a packet-based data system, which combines data, voice, and the Internet, it can transmit various data to the sites efficiently with up-to 32 channels [2]. With no active devices used in the network, it also saves power and money [3]. The GPON network extends coverage from the city to rural areas using a fiber network [4]. This technique covers large distances at low equipment cost. More remote areas can be reached by WiMax technology, which can be tightly integrated with GPON systems. This hybrid communication enables prompt data transmission to end users.

Multimedia data such as digital multimedia broadcasting (DMB) and multimedia files on the Internet have increased tremendously and now reach even hand-held devices, as shown as Figure 1-3. Inside the hand-held devices or computers, a copper-based printed circuit board (PCB) needs to handle the higher bandwidth data due to these increases [5]. This change in data volume will affect the overall communication channel, possibly causing a bottleneck in the established channels. The GPON system is one of the feasible technologies to accommodate these changes. From the central office, the GPON is connected to a higher data-rate backbone network, which is usually the Ethernet, whose data-rate can reach 10 Gbps. This GPON connected to the Ethernet works as the backbone for metro link as shown in Figure 1-4. This connection between the GPON and the Ethernet is through backplanes in servers or storage devices [6]. A high data rate (usually 10 Gbps) is applied between network accesses points. In this dissertation, two communication channels, the GPON based optical channel and the backplane channel, will be analyzed for their dispersive effects, and techniques for improving the signal integrity in these channels will be proposed.

The equalization concept is applied to the link between the Ethernet and the GPON central office in order to cancel inter-symbol interference (ISI) in the backplane to accommodate more data rates [7]. In the GPON link, this same concept is used to compensate for various dispersions in the optical domain, which occurs mainly in the fiber and laser [8]. Finite impulse response (FIR) type equalizers are chosen for the design of these applications.

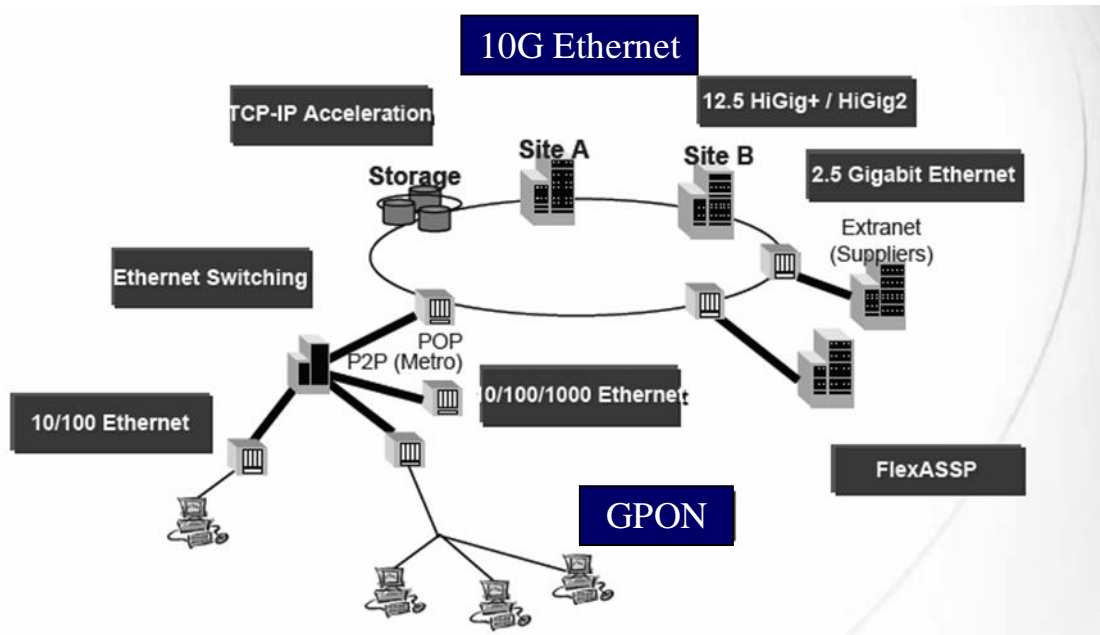


Figure 1-4. Metro communication link with GPON and the Ethernet.

For the adaptive operation of the equalization, designing a control loop for the equalizer is essential. One of the key elements in this loop is monitoring the performance of the equalizer in the channel to determine the tap coefficients of the equalizer. The proposed analog eye monitor achieves this function without complexity of a digital circuit block. Using different delayed signals and the subtract function gives the fall and the rise time of the equalized signal, which corresponds to the performance of the equalizer. According to the quality of the signal, the output of the eye monitor block gives the DC values, which are then used to estimate the performance of the equalizer and to adjust the condition of the equalizer for the optimum channel environment.

This dissertation investigates the channel impairment in the electrical and the optical signal. More specifically, channel characteristics on backplane channels are analyzed using S-parameter data. Channel characteristics of fiber optic cables are analyzed using the impulse response with the computed power penalty over the channel. These channel characteristics are measured to be used as design specifications. Among the various types of the equalization functions, the finite impulse response (FIR) type of equalizer is

selected for this work. This is because it is much simpler yet more effective compared to that of the other types. It can also be adapted easily using the feedback loop and the additional control block. A review of the different architectures in the literature will be presented in the following chapter.

A 10 Gbps data-rate signal through a 20 inch backplane is completely distorted by channel loss characteristics. The equalizer compensates for this loss in the channel and helps to extend the bandwidth in the existing hardware. A system simulation is performed for the given band-limited channels, and the optimum system specification is extracted for circuit design. Various types of delay lines are implemented in equalizers with silicon technology. Different technologies will be compared to show their benefits.

The FIR type equalizer can remove ISI in the GPON upstream links. ISI in the optical domain is created by dispersions from the fiber. This is the reason the equalizer in the optical domain is called an electronic dispersion compensator (EDC). As with the backplane system, GPON channel improvement with the equalizer is also simulated, and the GPON link is implemented in the lab to test the equalizer performance.

The FIR type equalizer is not optimum due to its summing point at one node when finer cancellation and higher bandwidth is needed. To extend the bandwidth of the equalizer, a distributed amplifier type is proposed. This is called a balanced delay line equalizer because its delay is positioned at the input and the output side of the amplifier cells. The distributed amplifier type equalizer is also designed to give backplane communication channels finer cancellation with a greater number of taps. Finally, a novel eye monitoring scheme is introduced to implement the adaptive operation of the optimizing coefficients of the equalizer. This eye monitoring scheme helps achieve adaptive operation of the equalizer system.

The proposed method for band limited channels provides a one-chip solution. This enables faster data transmission in the backplane and optical channel with the existing hardware, providing an attractive solution because of its simplicity and cost-effectiveness.

The original contributions and main focus of this dissertation include the following:

1. Development of the Electronic Dispersion Compensator (EDC) for 1.25 Gbps Gigabit Passive Optical Network (GPON) upstream links in a 0.18- μm CMOS technology.
2. Development of the balanced delay Feed-Forward Equalizer (FFE) with 0.18- μm CMOS technology for backplane channels.
3. Introduction the novel eye monitoring scheme with adjustable active delay line for the adaptive operation of the FFE.

This dissertation is organized as follows:

Chapter 1 introduces the motivation for this research and the origin of the problem for band-limited channels. Chapter 2 explains the details of band-limited channels (electrical and optical channels) and analyzes the characteristics of band-limited channels such as FR-4 (Flame Retardant) -based backplanes and the single mode optical fiber. The chapter then details the channel impairment factors such as ISI in backplanes and various dispersions in fibers. This measured characteristic of channels is used to decide the specifications of the circuits. Major specifications of the equalizer are the number of taps, the tap coefficients, and the amount of tap delay. The concept of equalization is also introduced here. Chapter 2 concludes by explaining the various techniques of equalization in order to compare the pros and cons of each topology and decide the optimum technique for the given communication channel.

Chapter 3 focuses on the equalizer design for 10 Gbps backplane communication channels. Two approaches are implemented for the specific channels. The first approach uses a passive delay line with CMOS 0.18 μm technology. This delay line utilizes an L-C ladder structure as an artificial transmission line to achieve a delay of 100 ps. The other approach uses propagation delay through active devices. Because

passive devices consume a lot of space, active devices are a more economical solution with only a marginal increase in power consumption. Another advantage of the active delay line approach is that it can compensate for the loss through passive devices. The active delay line approach is implemented in CMOS 0.18 μm technology and BiCMOS 0.25 μm technology, which has higher fit compared to the CMOS process. A system level analysis with measured channel data is performed to demonstrate the impact of the equalization prior to circuit designs. The chapter then presents the detailed IC implementation issues, focusing on circuit level design details. Chapter 3 concludes by presenting measurement results demonstrating performance improvement with the actual backplane communication channel for 10 Gbps data.

Chapter 4 presents an electronic dispersion compensator (EDC) for 1.25 Gbps GPON upstream links. GPON upstream links suffer from the noise of the Fabry-Perot laser and fiber. To compensate for this loss, the equalization technique is employed in the electrical signal domain. For area-efficiency, the active delay line approach is used to achieve 278 ps delay with four tap spacing in CMOS 0.18 μm technology. System simulations are also performed to estimate the impact of the EDC. For the measurement, the GPON upstream link in the lab environment is built in conjunction with the IC measurement platform.

Chapter 5 presents the new balanced delay line structure of the equalizer, which is based on the distributed amplifier structure in order to achieve higher bandwidth. This circuit is also fabricated in CMOS 0.18 μm technology. The chapter then shows the measurement for the backplanes with 3 Gbps signal to verify the performance of the equalizer.

Chapter 6 introduces an eye monitoring scheme using the fall and the rise times of the signal. This block is critical for adaptive operation of the equalizer to change values to the optimal point.

Finally, chapter 7 summarizes the dissertation and provides guidance for future research possibilities.

CHAPTER II.

BAND-LIMITED CHANNELS AND EQUALIZATION

2-1. BAND-LIMITED CHANNELS

2.1.1. Backplane Channel

The 10 Gbps Ethernet is connected to the GPON through backplane links. The backplane link is a high-speed differential, point-to-point serial link between chips on a line card and a chip on another line

card. Figure 2-1 shows a picture of the typical backplane. The high-speed transceiver chipsets are mounted on the line cards. These line cards are plugged into the printed circuit board (PCB) backplane board through the high-speed connectors. The multi-giga bit per second data signals are transmitted through the parallel PCB traces on the backplane. In this signaling environment, the passive physical components are the line card, the backplane PCBs, and the backplane connectors. The flame-retardant (FR)-4 is the most widely used dielectric material in the legacy backplane boards.

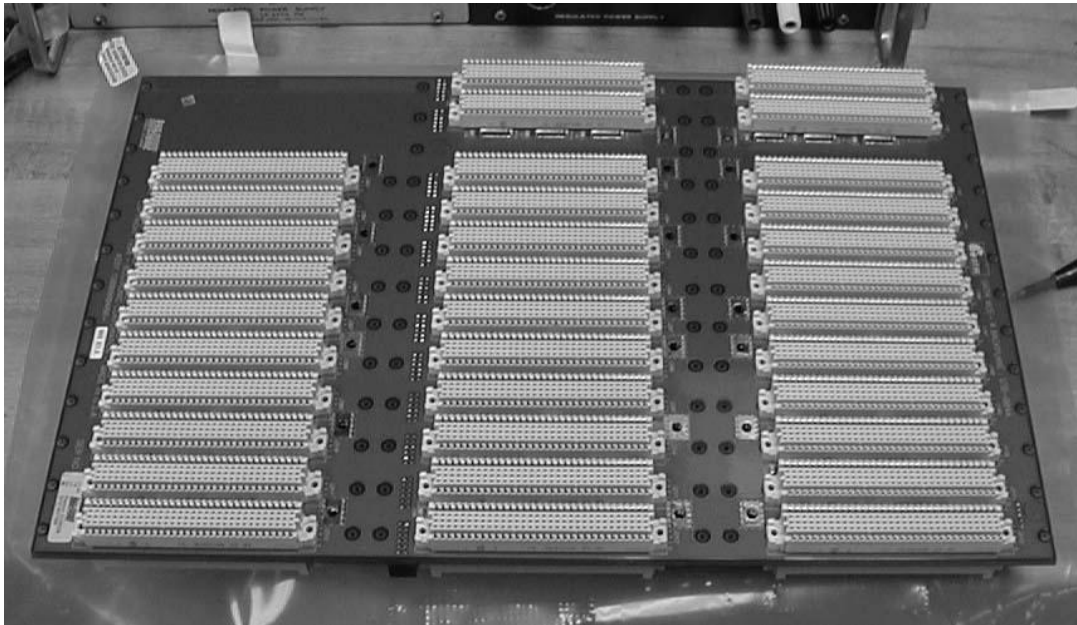


Figure 2-1. Picture of the typical backplane channel.

Channel impairment elements in backplanes are DC loss, a skin effect, and dielectric. The DC loss is related to the resistivity and the area of the conductor [9].

$$R = \frac{\rho L}{A} = \frac{\rho L}{Wt},$$

where R is the total resistance of the line, ρ the resistivity of the conductor material in ohm-meters, L the length of the line, W the conductor width, t the conductor thickness, and A the cross-sectional area of the signal conductor.

The skin effect is a physical phenomenon related to high-frequency transmission on a wire. It is the tendency of an alternating electric current (AC) to distribute itself within a conductor so that the current density near the surface of the conductor is greater than that at its core. That is, the electric current tends to flow at the "skin" of the conductor. This skin effect, which is due to eddy currents set up by the AC current, causes the effective resistance of the conductor to increase with the frequency, resulting in increased signal attenuation at higher frequencies. The amount of penetration into the material, which is known as the skin depth, is shown in the equation below:

$$\sigma = \sqrt{\frac{2\rho}{\omega\mu}} = \sqrt{\frac{\rho}{\pi f\mu}},$$

where ω and μ are the angular frequency and the permeability of free space, respectively, and ρ is the resistivity of the metal. The effective resistance R is given as $R = \frac{\rho}{\sigma}$ and the attenuation α_s is expressed as

$$\alpha_s = \frac{R}{Z_0 W} = \frac{\sqrt{\pi\mu\rho f}}{Z_0 W} \quad (2.1)$$

where Z_0 is the characteristic impedance of the conductor and W is the width of the conductor.

As the frequency increases over 1 GHz, the dielectric loss becomes another dominant loss factor in legacy backplane applications. When dielectric losses are accounted for, the dielectric constant of the material becomes a complex value, as shown in the equation below:

$$\epsilon = \epsilon' - j\epsilon''$$

where the imaginary portion represents the losses and the real portion is the typical value of the dielectric constant.

Subsequently, $1/\rho = 2\pi f \epsilon''$ becomes the equivalent loss mechanism, where ρ is the effective resistivity of the dielectric material and f is the frequency. The typical method of loss characterization in dielectrics is by the loss tangent shown in the equation

$$\tan|\delta_d| = \frac{1}{2\rho\pi f \epsilon'} = \frac{\epsilon''}{\epsilon'}$$

Dielectric loss as a function of the frequency is expressed as below:

$$\alpha_D = \pi f \tan \delta_d \sqrt{\epsilon'} \quad (2.2)$$

If the frequency falls low enough (usually below 1 Gbps), the losses due to dielectric absorption at that frequency are swamped by the skin-effect losses. As the frequency is increased, however, the skin-effect loss grows only in proportion to the square root of the frequency, while the dielectric loss grows at a faster rate in direct proportion to the frequency. Above a certain frequency, the dielectric loss equals and then exceeds the skin-effect loss. Due to this phenomenon, as shown in Figure 2-2 (based on equations 2.1 and 2.2); the dielectric loss becomes a dominant factor when the frequency of the signal is above 1 Gbps. All these elements contribute to signal integrity degradation in the FR-4 backplane [10, 11].

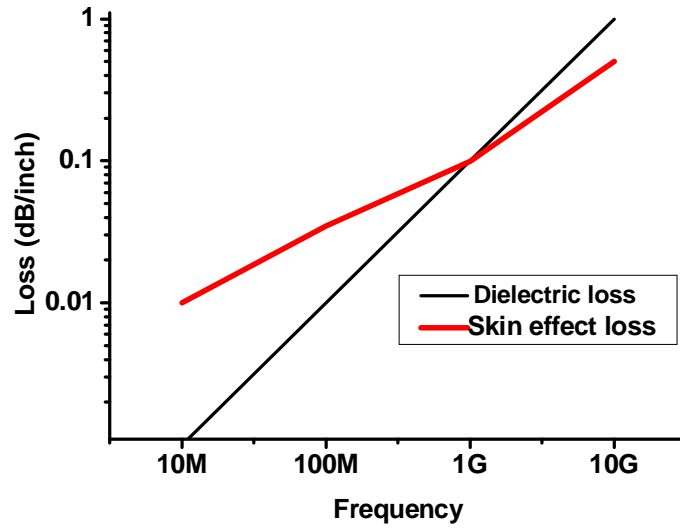


Figure 2-2. Relation between skin effect loss and dielectric loss in the frequency domain.

Channel impairments in backplanes resulting from the DC loss, the skin effect and the dielectric loss are dramatically increased when data rates approach several giga-bits per second. The relations between loss characteristics are shown in Figure 2-3. Backplane channels have low pass filter characteristics, resulting in increased rising time and falling time of the transmitted signal. The increased rising time and falling time causes inter-symbol interference (ISI), in other words, dispersion in the channel impulse response. This dispersion occurs in transmission lines that have phase variations. These phase variations translate to group delay, which is expressed as the derivative of phase variations and increases with the frequency and to a fraction of the unit interval (UI) width as the data rate goes beyond 4 Gbps. The formula of the group delay can be expressed as

$$\tau_g = -\frac{d\phi}{d\omega}$$

where τ_g is group delay, ϕ the phase shift and ω the frequency.

As a result, phase variations also contribute to ISI. ISI is a signal-dependent, sensitivity-reducing impairment. ISI is the main source of signal distortion in digital communication systems.

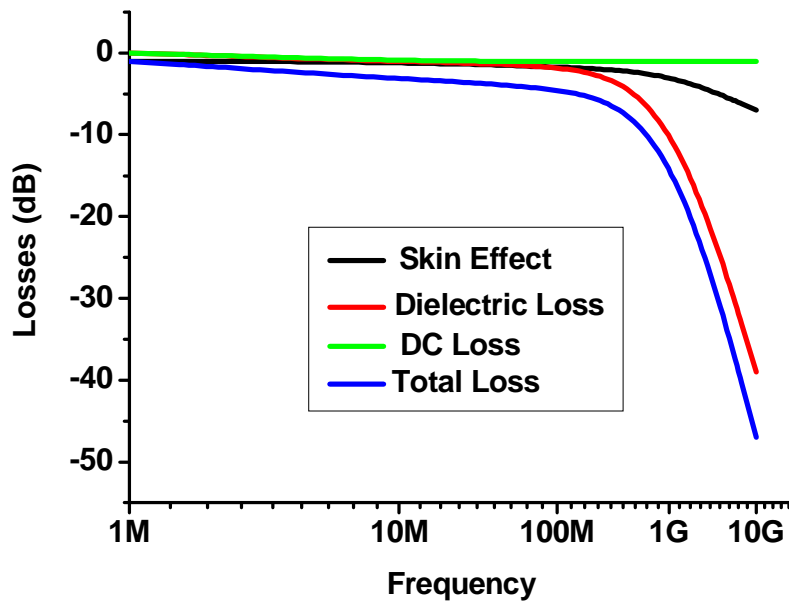


Figure 2-3. Backplane loss relations in the frequency domain.

As for the time domain measurement, Figure 2-4 shows an eye diagram that contains important information such as noise, noise margin, and jitter in its pattern. Noise is recognized by the thickness of the top and bottom lines of the eye diagram. The noise margin is interpreted by the eye opening in the center of one-bit unit interval. This eye opening can be used as a measure for signal integrity. If the signal has a wider eye opening, it also has better noise margin. Jitter is the width at the intersection between each eye pattern. Jitter is categorized as either random jitter or deterministic jitter. Random jitter, also called Gaussian jitter, is unpredictable electronic timing noise. It typically follows a Gaussian distribution or Normal distribution. It is believed to follow this pattern because most noise or jitter in an electrical circuit is caused by thermal

noise, which has a Gaussian distribution. Another reason for random jitter's distribution is the central limit theorem, which states that the composite effect of many uncorrelated noise sources, regardless of the distributions, approaches a Gaussian distribution. One of the main differences between random and deterministic jitter is that random jitter is unbounded, but deterministic jitter is bounded. Deterministic jitter is predictable and reproducible. Its two sources are insertion loss of the channel and group delay variations. Only deterministic jitter can be addressed with an equalizer. The peak-to-peak value of this jitter is bounded, and the bounds can easily be observed and predicted. Periodic jitter, data-dependent jitter, and duty-cycle dependent jitter are all types of deterministic jitter. In Figure 2-4, the eye opening is expressed as $\frac{a}{b}$, and jitter is expressed as $\frac{c}{d}$.

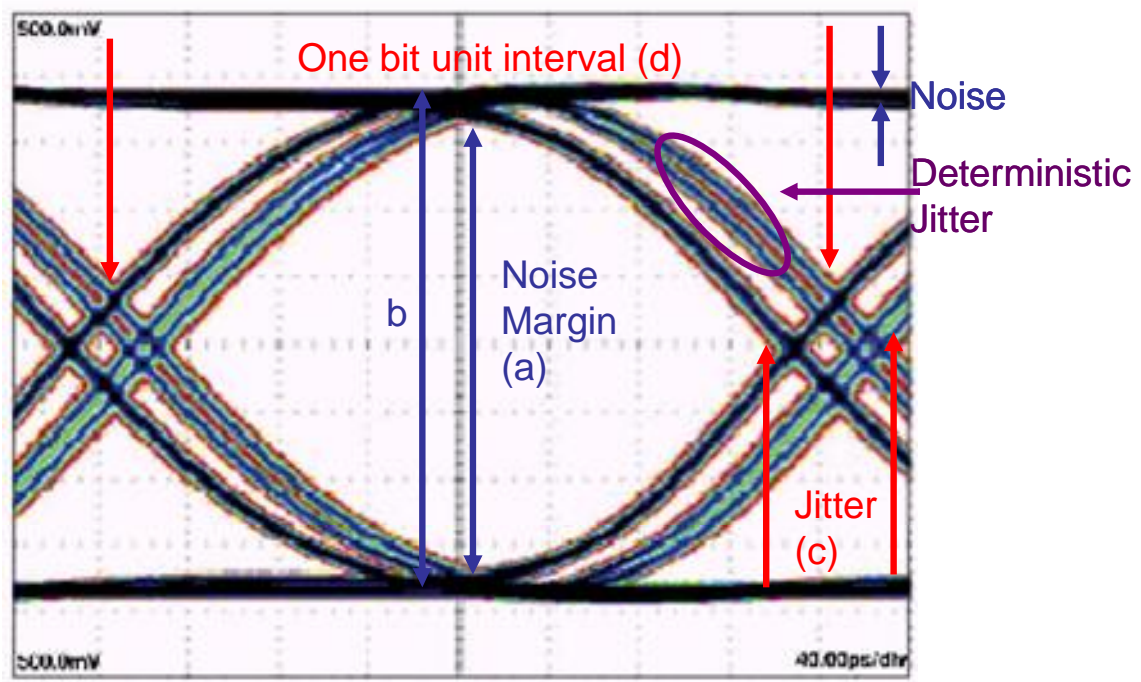


Figure 2-4. Measured eye diagram.

Another representation of jitter is provided by the bathtub plot shown in Figure 2-5, so named because its characteristic curve looks like the cross-section of a bathtub [12]. It is a graph of BER versus sampling points throughout the unit interval. It is typically shown with a log scale, which illustrates the functional relationship of sampling time to bit-error ratio. When the sampling point is at or near the transition points, the BER is 0.5 (equal probability for success or failure of a bit transmission). The curve is fairly flat in these regions, which are dominated by deterministic jitter mechanisms. As the sampling points move inward from both ends of the unit interval, the BER drops off precipitously. These regions are dominated by random jitter mechanisms, and the BER is determined by the sigma of the Gaussian processes producing the random jitter. As expected, the center of the unit interval provides the optimum sampling point. The curves of the bathtub plot readily show the transmission-error margins at the BER level.

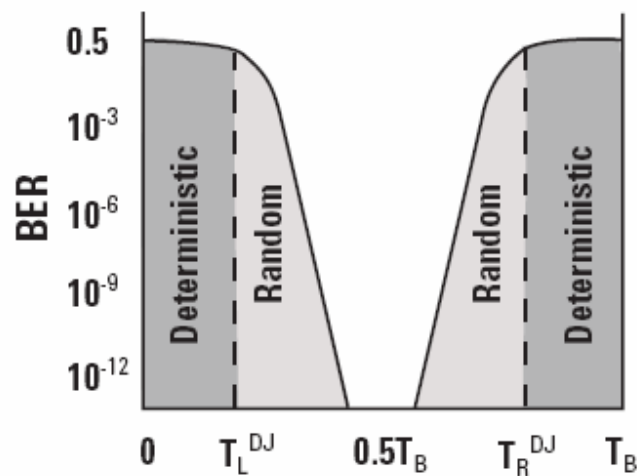
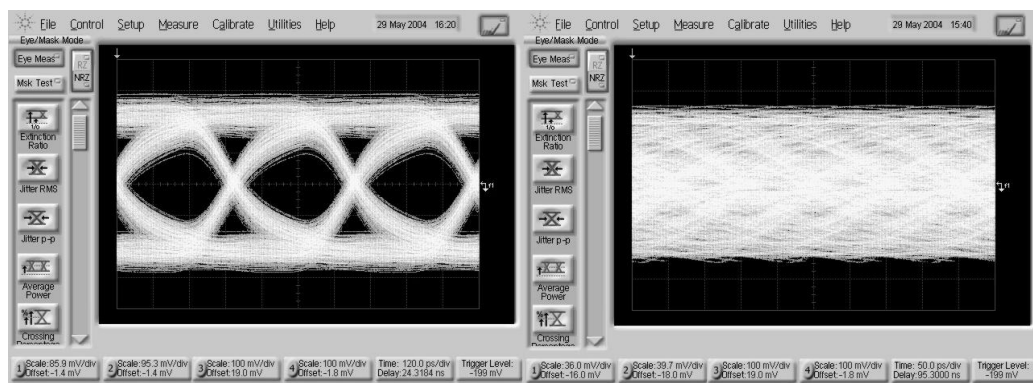


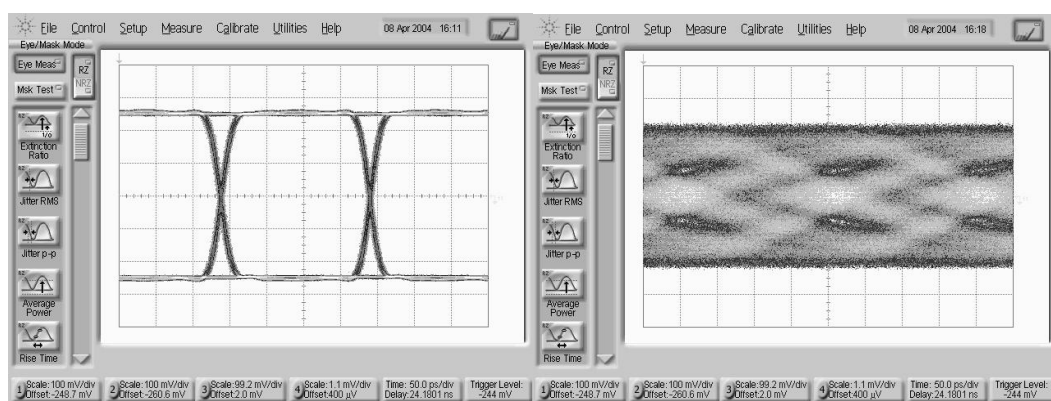
Figure 2-5. Bathtub plot.

ISI reduces the eye opening and increases the bit error rate. This problem is exacerbated by the fact that ISI worsens with a higher data rate and longer distance. The effect of ISI of different data rates is shown in Figure 2-6 (a), (b). The effect of the ISI on different distances is shown in Figure 2-6 (c) and (d).



a)

b)



c)

d)

Figure 2-6. Eye diagrams of different data rates a) 2.5 Gbps b) 10 Gbps and different channel distances
c) 0-inch d) 16-inch backplane.

2.1.2. GPON Channel

A GPON system is a point-to-multipoint network architecture deploying optical access lines between the carrier's central office and customer sites. In a GPON system, the content is distributed from the central office, the optical line termination (OLT), to an optical network unit (ONU) at the customer's premises. A GPON system uses passive optical splitters to distribute the content to multiple premises, depending on the distance from the OLT to the ONU, the total fiber length can vary between 5 km and 20 km [13]. The system diagram of a GPON system is shown in Figure 2-7.

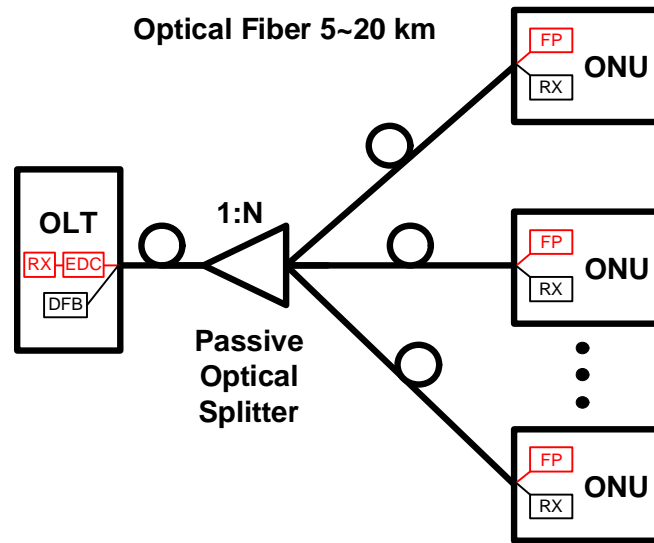


Figure 2-7. Block diagram of the GPON link.

Although GPON link channels are not as high speed as backplane channels, they also face the channel impairment problem. The performance of fiber optic transmission is often limited by one form or another of optical dispersion. ISI induced by these dispersions is exponentially increased with the distance and data-rate and results in a power penalty of the system.

The traffic from the OLT to the ONU, the downstream path, uses a 1550 nm window. The upstream path, the traffic from the ONU to the OLT, uses a 1310 nm window. This allows for two-way traffic on a single optical fiber, which uses wavelength-division multiplexing (WDM) to accommodate simultaneous upstream and downstream communication paths and to eliminate crosstalk between the paths. It uses one wavelength for downstream traffic and another for upstream traffic on a single nonzero dispersion shifted fiber (ITU-T G.652). Fiber loss is dependent on the wavelength of the signal, as shown in Figure. 2-8. The downstream path utilizes the higher wavelength (1550 nm) for a higher than 2.5 Gbps data rate because this wavelength exhibits the lower loss of 0.19 dB/km. The upstream path utilizes the lower wavelength (1310

nm) and exhibits a loss of approximately 0.35 dB/km. Recently, the ITU-T approved the GPON standard with a 1.25/2.5 Gbps cumulative transmission speed (FSAN ITU-T G.984 standard).

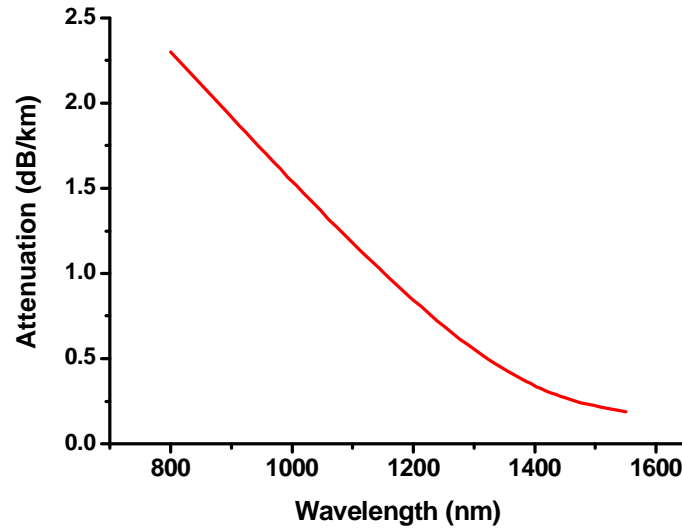


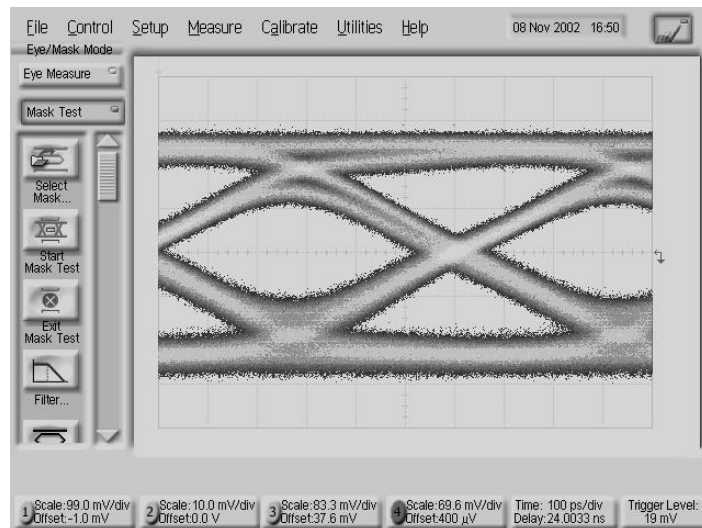
Figure 2-8. Block diagram of the GPON link.

A major limiting factor in a GPON system that arises when Fabry-Perot (FP) lasers are used in the upstream path (1.25 Gbps) at gigabit transmission speed is mode partition noise (MPN) of the Fabry-Perot lasers in conjunction with dispersion in standard fibers [14]. Even though the downstream path carries a higher data rate (2.5 Gbps) than the upstream path, it is less susceptible to the noise because of the use of the stable distributed feedback (DFB) laser. Analysis of Fabry-Perot laser will be discussed in Chapter IV along with an analysis of general fiber dispersion.

There are three major types of dispersion in optical fibers: chromatic dispersion (CD), differential modal delay (DMD), and polarization modal dispersion (PMD) [15]. CD and PMD are the main sources of noise in a single-mode fiber (SMF), while DMD is the major source in a multi-mode fiber (MMF). Since the GPON system utilizes SMF, the focus here will be on CD and PMD. CD occurs because different

wavelengths of light travel through the fiber at different speeds. Since the different wavelengths of light have different velocities, some wavelengths arrive at the fiber end before others. This delay difference is called the differential group delay, which leads to pulse broadening and eventually ISI. PMD is a modal dispersion by the random spreading of optical pulses. This spreading is caused by the different speeds of two different polarizations of light in the waveguide due to asymmetries.

The dispersion effects on the optical system can be better understood with the use of eye diagrams, which are the result of measuring varying dispersion rates within a fiber. The eye diagram for PRBS 1.25 Gbps before the signal enters the fiber is shown in Figure 2-9 (a) and the eye diagram representing the signal after it passes through the fiber is shown in Figure 2-9 (b). These eye diagrams clearly show that fiber dispersions clearly worsen signal integrity. The measured impulse response with the fiber dispersion is shown in Figure 2-10.



a)



b)

Figure 2-9. Eye diagrams a) without fiber dispersion b) with fiber dispersion.

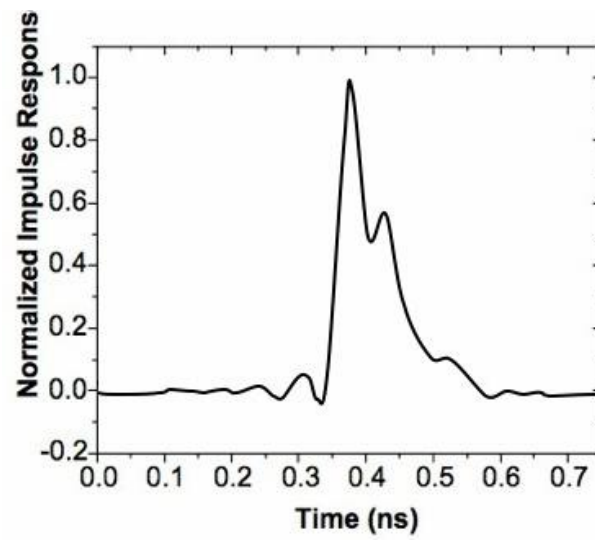


Figure 2-10. Measured impulse response with the dispersion.

2-2. CONCEPT OF EQUALIZATION

As discussed in the previous chapter, two communication links have different sources of ISI. One of these sources is the band-width limitation in the frequency domain of the backplane channel. For the GPON channel, the cause of ISI is optical dispersions from the fiber with a Fabry-Perot laser. Even though the causes for ISI differ, performance in both these channels can be improved by applying the same technique, which applies the concept of equalization for two different channels.

The basic concept of the equalizer is to compensate for any signal distortions or any general losses resulting from channel characteristics. A simple linear equalizer has the following equivalent mathematical transfer function:

$$G_E(f) = \frac{1}{C(f)} = \frac{1}{|C(f)|} e^{-j\theta_c(f)}$$

where $C(f)$ is the channel characteristics and $G_E(f)$ is the equalizer transfer function characteristics [16, 17]. The amplitude response of the equalizer is $|G_E(f)| = 1/|C(f)|$ and its phase response is $\theta_E(f) = -\theta_c(f)$. As the equalizer transfer function is the inverse form of the channel, the equalizer should completely eliminate ISI caused by the channel [18].

In the backplane channel, the loss in the channel becomes greater as the data rate increases. Especially at 10 Gbps, ISI due to the loss deteriorates the signal, resulting in a completely closed eye diagram. An equalization technique compensates for the frequency-dependent channel loss characteristics. As shown in Figure 2-11 (a), the band-limited channel has a low-pass frequency response. Specifically, high-frequency components of the input signal experience larger loss than the lower-frequency components around DC. The equalization technique restores the high-frequency component of the original transmitted signal.

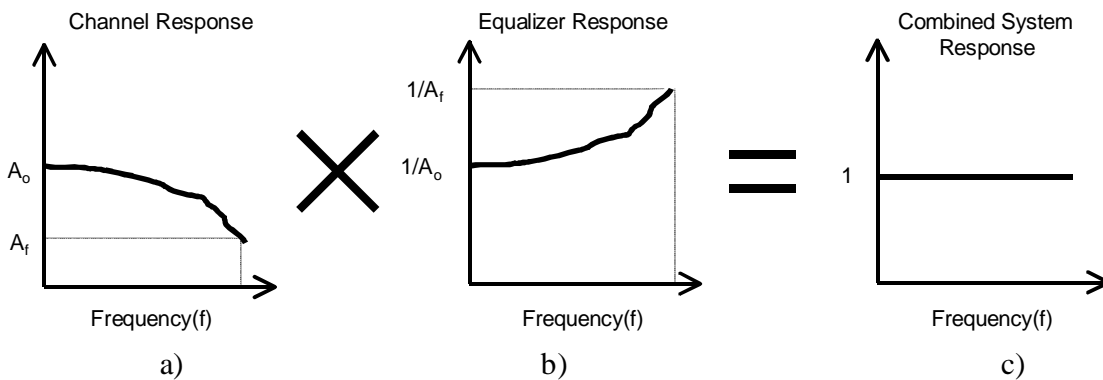


Figure 2-11. Conceptual illustration of equalization in the frequency domain a) channel response, b) equalizer response, c) equalized response.

The frequency response of the equalizer has larger gain values at the high frequencies compared to gain values for the low frequencies around DC, as shown in Figure 2-11 (b). After equalization, the frequency response of the system becomes flat through the desired frequency range, as shown in Figure 2-11 (c). This new transfer function has lower loss at the higher frequency than the original transfer function had.

From the time-domain perspective, the concept of the impulse response helps to explain the problem. As shown in Figure 2-12, optical dispersion from the fiber and the laser makes the impulse response wider than its original shape. The width of the impulse response indicates the degree of signal power dissipation in the time domain for a given pulse width. These are called the pre-cursor and post-cursor ISI, depending on their respective locations. A symbol is defined as a state or significant condition of the communication channel that persists for a fixed period of time. In this case, the effect of the past and future symbol on the current symbol is ISI. Pre-cursor ISI is caused by the past symbol and post-cursor is caused by the future symbol. This phenomenon is not desirable because the previous symbols have an effect on the next symbols and, as a result, distort the signal, decreasing the reliability of the communication by increasing the overall bit error rate.

This channel can be improved if tap coefficients of the gain cells of an equalizer add positive or negative gain values to remove post- and pre-cursor ISI, as shown in Figure 2-12. Spacing between gains can be achieved by using delay cells according to the data rate of the system. Therefore, an equalizer can be regarded as a spectrum-shaping filter to narrow the channel impulse response to bring it back to its original transmission pulse width

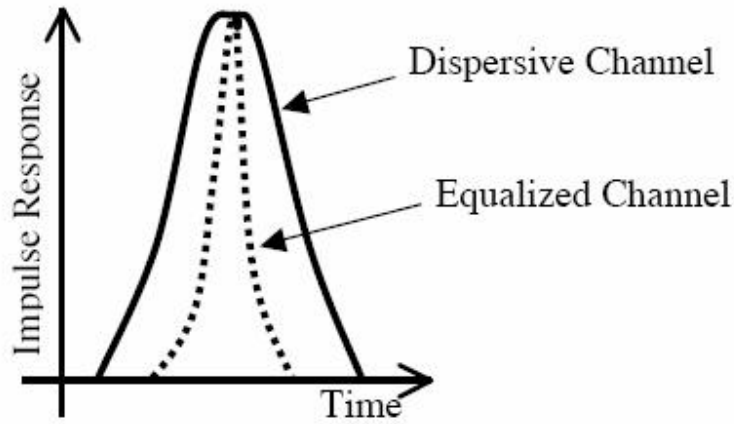


Figure 2-12. Impulse responses before and after equalization.

The two types of equalization are linear equalizers and non-linear equalizers. For a linear equalizer, the current and the past values of the received signal are linearly weighted with equalizer coefficients and combined to produce the output. This type of equalizer, which is also called the finite impulse response (FIR) type feed-forward equalizer (FFE), compensates for ISI with adjustable tap-coefficients, as shown in Figure 2-13. It consists of a delay line, gain cells, and a summing node. The transfer function of the equalizer is expressed by $y(t) = \sum_{i=0}^n A_i x(t - i\tau)$, where A_i is the weight from gain cells and τ is the delay amount of one delay cell. The value of the tap (n) number and that of the delay amount (τ) are extracted from the system simulation, which will be explained later. There are two ways to determine tap coefficients of linear equalizers. The first way to compute the coefficients is with the zero forcing equalizer, which has the inverse channel transfer function characteristic. Although this method can completely remove ISI, it significantly increases the additive noise in the channel. From the point-of-view of minimizing error probability, allowing some residual ISI is advantageous if this can reduce the overall noise power. This alternative solution is called the minimum-mean-square-error (MMSE) algorithm, where the tap values are

optimized to minimize both the power in residual ISI and the additive noise in the channel [19]. A comparison of the frequency responses between the application of zero-forcing and MMSE is shown in Figure 2-14.

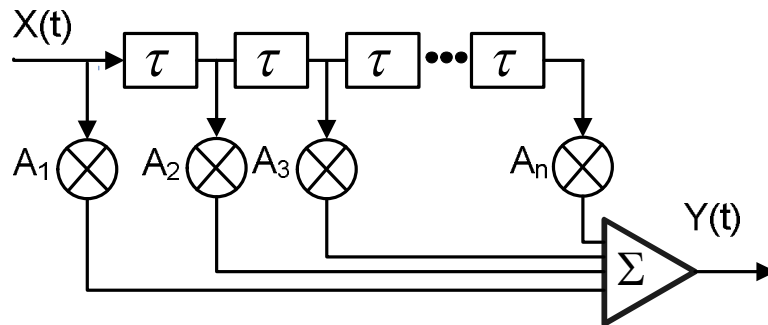


Figure 2-13. Block diagram of the FIR filter

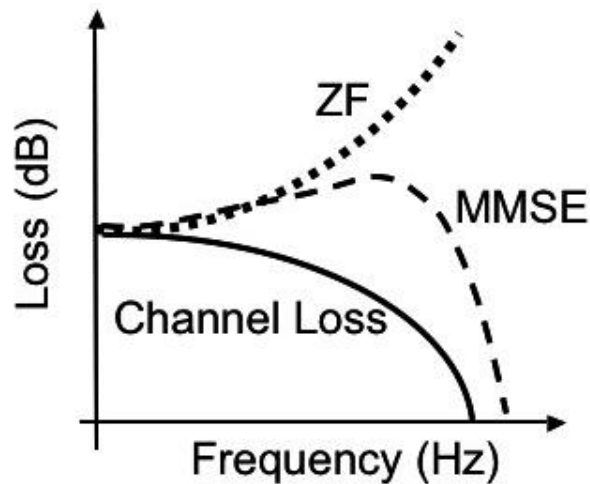


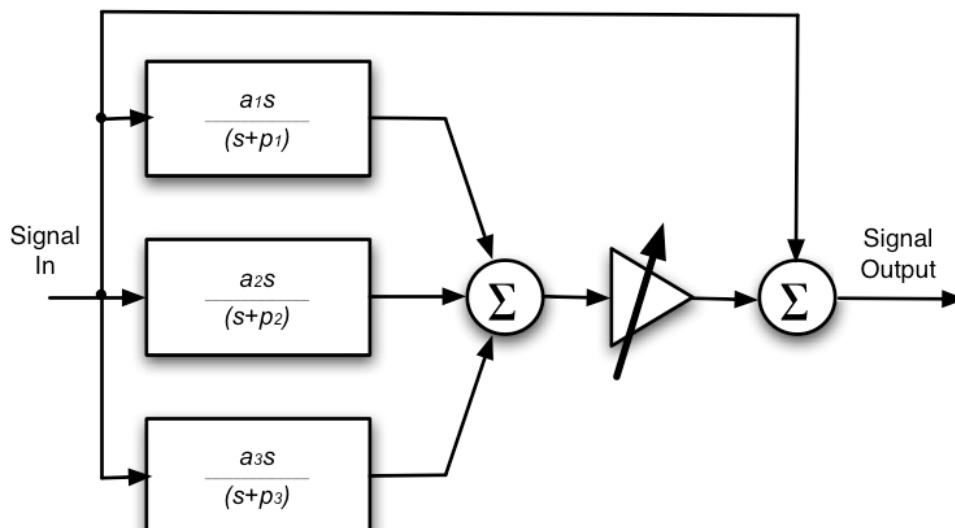
Figure 2-14. Frequency responses of band-limited channel, ZF-LE, and MMSE-LE

Other design parameters are the number of taps and the amount of the delay. A greater number of taps means greater cancellation of ISI, but this comes at the cost of the power and the complexity of the equalizer. Also, the bandwidth is the factor that needs to be considered before deciding the number of taps.

The amount of the delay is decided together with the number of taps because the space between delay cells is distributed evenly in the UI.

For the FFE, the equalizer block can be placed on the receiver side or the transmitter side. Transmitter side equalization has an advantage in implementing the digital control with the FFE. However, placing the FFE on the transmitter side also boosts high-frequency components with pre-emphasis at data transition, which can increase the near-end crosstalk between connectors. Another disadvantage to this technique is that it requires the information from the receiver side for adaptive operation. For these reasons, receiver equalization is a better candidate for adaptive equalization.

Another type of equalizer, one designed specifically for a cable channel, is the bode equalizer. Just as a cable channel can be modeled with a simple low pass filter transfer function, a cable equalizer can be implemented with a combination of a high pass filter with several poles as design parameters and the variable gain controller, as shown in Figure 2-15 [20]. The variable gain can be controlled via an MMSE or other algorithms for adaptive operation depending on channel conditions. Compared to other types of equalizers, the cable equalizer is practical to implement by analog continuous time signal processing because it does not need a timing recovery circuit like a clock or a data recovery (CDR) block. The bode equalizer is can be easily applied to the cable channel, but its gain variation is not as wide as the FIR type equalizer.



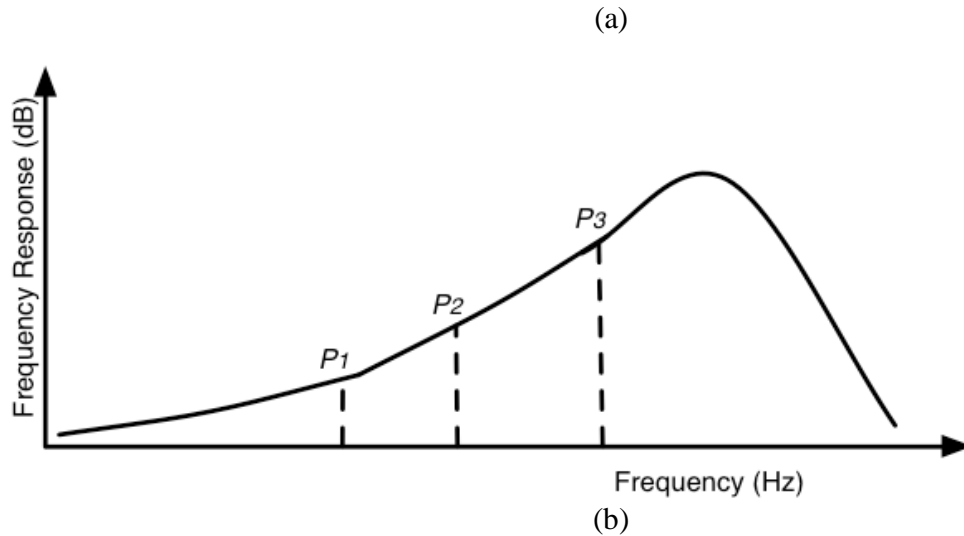


Figure 2-15. (a) Block diagram for the simple cable equalizer and (b) corresponding frequency response indicating pole locations.

As described in the previous section, linear equalizers are very effective on channels, such as wire line telephone channels, where ISI is not severe. However, in channel environments where ISI is severe, the linear equalizer is not powerful enough to compensate for the noise. Such channels are often encountered in mobile radio channels, such as those used for cellular radio communication. Another solution for channel improvement is more advanced techniques that employ decision feedback equalizers (DFE) for non-linear channel impairments [21]. A DFE is a non-linear equalizer that employs previous decisions to eliminate ISI caused by previously detected symbols on the current symbol.

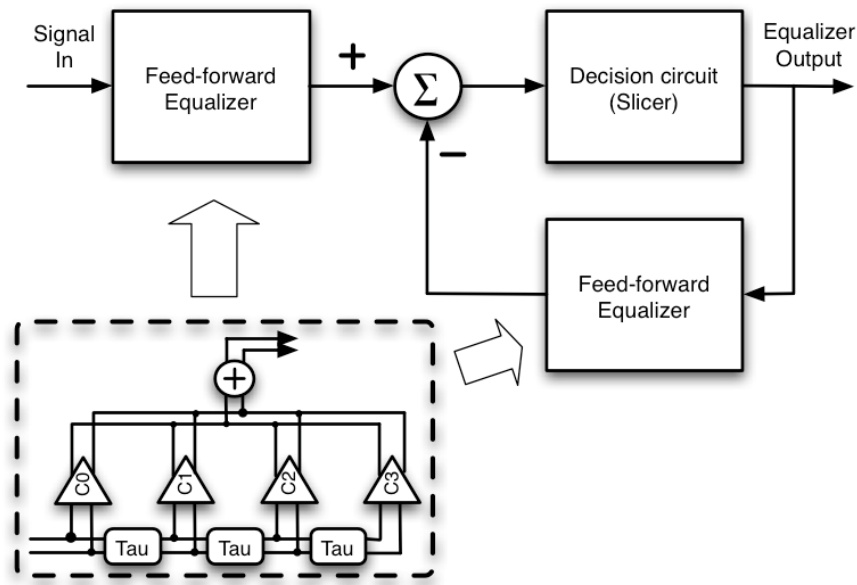


Figure 2-16. Block diagram of the conventional DFE.

The DFE is typically used in conjunction with a linear FFE as shown in Figure 2-16. Even though the linear FFE alone can be used to cancel ISI, the combination of the linear FFE and the DFE has significantly better performance. The principal reason for this improvement is that the DFE uses a linear combination of noiseless binary decisions to eliminate some of the ISI and does not add noise at the input of the decision circuit. The linear FFE amplifies the high-frequency portion of the signal and the noise to cancel ISI, which is not compensated for by DFE. The result is that the noise enhancement of the linear FFE in conjunction with DFE is less than that when the linear FFE alone is used. Recently, the DFE has been reported as a good candidate for backplane channel equalization, where the near-end-crosstalk is severe [22]. One potential problem with a DFE is error propagation [23, 24]. If the DFE outputs an incorrect decision, the error will propagate through the feedback filter and increase the probability that another incorrect decision will be made.

Equalization may also be performed in the digital domain by means of controlled digital FIR filters. Continuous time equalization techniques have some advantage over their discrete time counterparts.

Because the received signal needs to be sampled and quantized with an analog-digital converter (ADC) before equalization, area and power consumption increases. Even for a multi-Gbp signal, ADCs are limited by their transistor switching speed and the time needed to convert the small analog signal to the digital voltage level. The use of an ADC itself complicates timing recovery in the signal path [25]. Therefore, subsequent discussions will address equalization by means of analog signal processing.

CHAPTER III.

EQUALIZATION FOR BACKPLANE CHANNELS

3-1. SYSTEM SIMULATION FOR 10 GBPS BACKPLANE CHANNEL

For accurate system simulation, the equalizer simulator is implemented using the MATLAB program. First, the frequency data of the backplane channel is measured using S-parameters. S-21 data, which are measured through different backplane channel lengths, are shown in Figure 3-1. As shown in the figure, backplane loss becomes severe when the distance and the frequency increase. Using this S-parameter data, the simulator extracts the impulse response of the channel. Then the pseudo random bit sequence (PRBS) 23 signal is fed into the channel in the simulator, and the output of the channel is extracted using measured S-21 data. By using a given tap number, the unit delay is also determined according to the channel. Optimum tap coefficients for various band-limited channels are extracted with the use of impulse response information. Tap coefficients are calculated for optimum equalization using the MMSE algorithm, as

mentioned in the previous section, which algorithm can suppress the overall noise. The comparative outputs of the simulated equalizer are shown in the eye diagram in Figure 3-2, with a) the eye diagram before equalization and b) the eye diagram after equalization. By this simulation, four tap numbers are extracted, resulting in a unit delay of 33 ps, which is one third of the 10 Gbps symbol rate for the measured backplane channel.

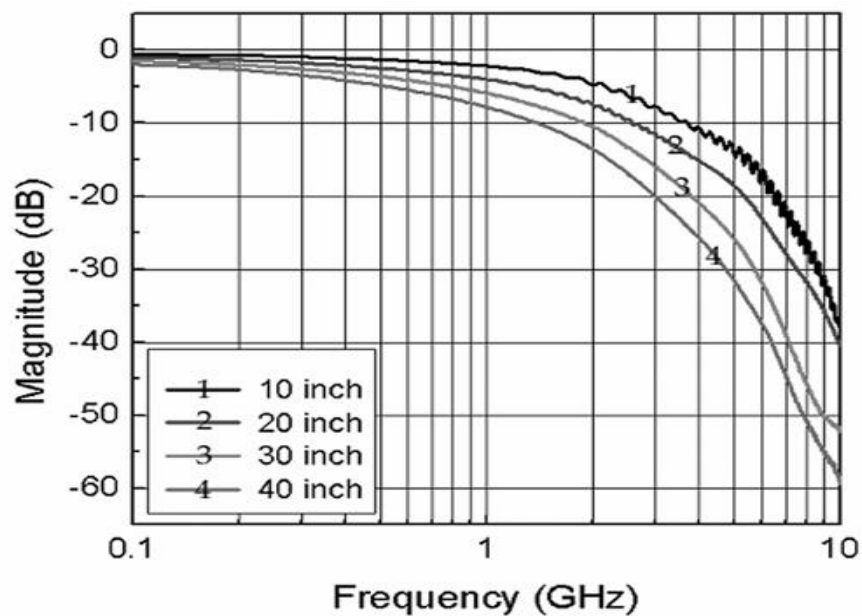
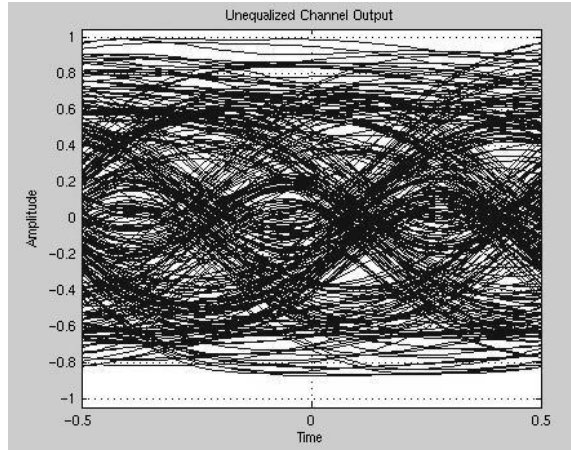


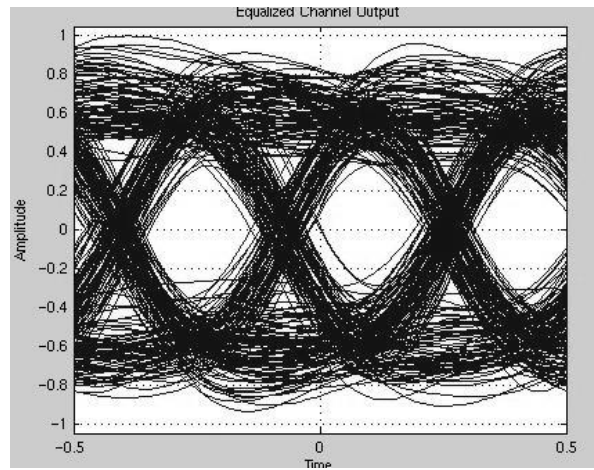
Figure 3-1. Measured S21 data of the backplane.

Extracted tap coefficients are -0.6847, 0.9275, 1.000, -0.8362 for one particular backplane channel environment.

Using this system analysis, we can predict the equalizer performance and extract the tap coefficients from the specified channel before the implementation of equalizers.



a)



b)

Figure 3-2. Eye diagram of a) before equalization and b) after equalization.

3-2. FFEs WITH DIFFERENT DELAY LINE STRUCTURES

To investigate the feasibility of the FFE at the 10 Gbps data-rate signal and compare the different structures of the FFE, we implement two different types of FFEs. One is the delay line with passive

components and the other is the delay line with active components. Each FFE follows the tapped-FIR filter structure of a linear transversal equalizer as shown in Figure 3-3. Fractionally spaced delays are obtained with a four-tap delay line which is determined from the system simulation. Because the buffered variable gain cells have external controls, they can adjust the tap weights. In order to operate with sufficient bandwidth for the given data rate (10 Gbps), the chain is restricted to four taps. This implies $T_s/3$ tap spacing, where T_s is the symbol duration, along with a matched termination at the end of the chain to suppress the reflection. The entire signal path is executed in differential mode. Variable tap gain is implemented in the form of the Gilbert cell, which acts as a V-I converter and sums the signal currents. The tail current of the differential pair is switched between the two arms in accordance with a control signal that determines both the magnitude and polarity of the gain. Passive loads are used rather than active ones to maximize small-signal bandwidth [26].

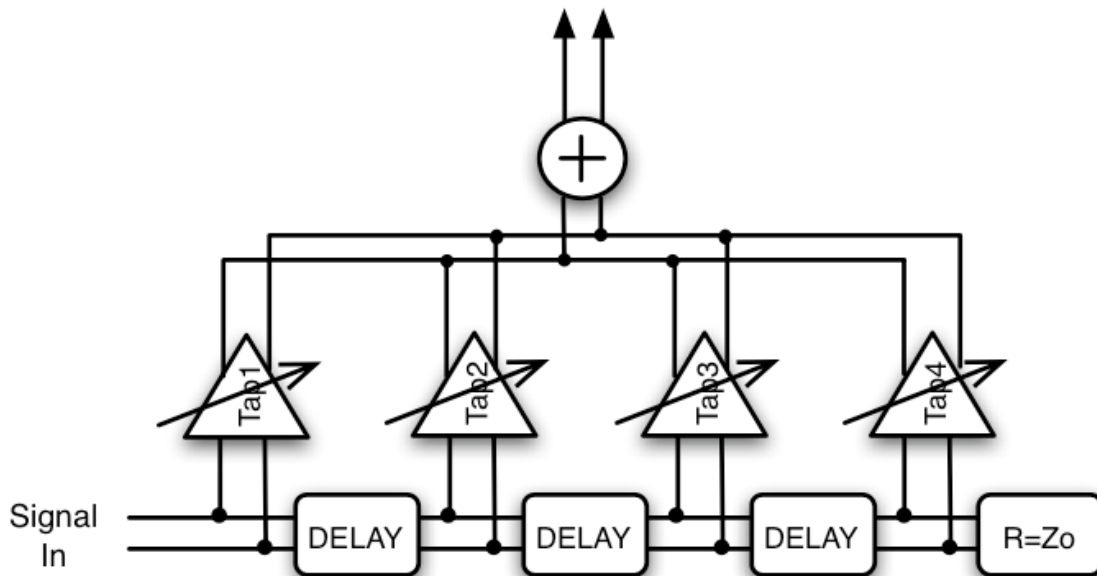


Figure 3-3. Block diagram of the FIR filter

A. Passive delay line FFE

Variable tap gains are needed to achieve opposite polarity gain values to cancel ISI. The variable gain amplifier (VGA) using Gilbert-cell architecture is adopted to meet this requirement as shown in Figure 3-4. Outputs of VGAs are summed at the one common resistor load. Because the current summing is done at one node, this common load has four times the DC current than that of the one VGA.

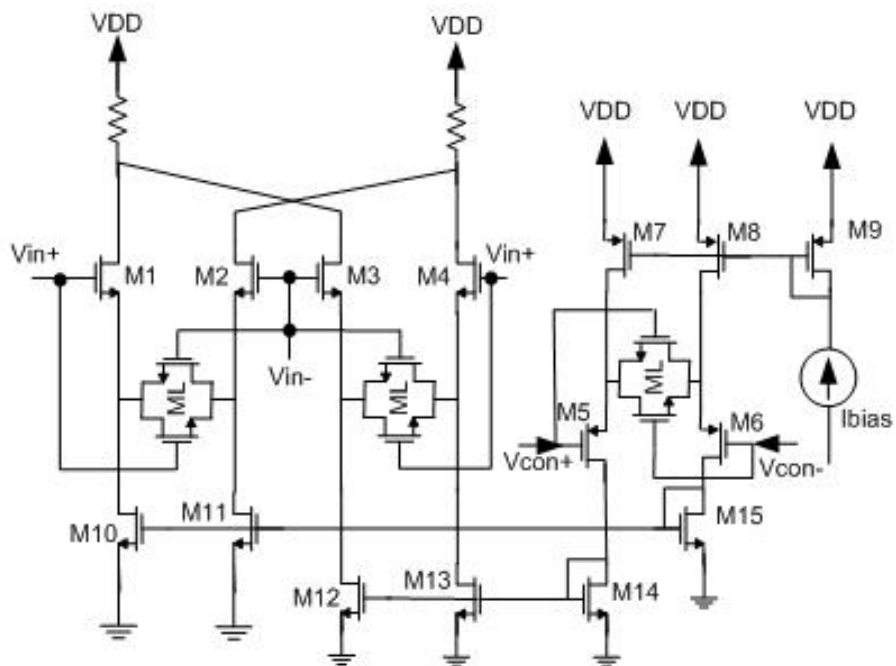


Figure 3-4. Schematic of the VGA.

This phenomenon causes a voltage headroom issue because of the significant voltage drop at the resistor summing load. If voltage is too low on the drain side of the VGA, transistors (M1~M4) in the VGA will be forced to the triode region due to the lack of voltage headroom.

The voltage headroom can be improved if the gain control circuit is folded with a current steering block using a PMOS differential pair (M7, M8). Control voltage is not directly applied to the differential pair below the common source. Instead, control voltages, V_{con+} and V_{con-} , are applied to M5 and M6 to provide the bias currents proportional to the control input. This modified architecture reduces the total number of stacked devices, thereby alleviating the headroom condition. Active degeneration transistors (ML) are added between divided common source pairs to improve gain linearity [27].

Figure 3-5 shows the overall VGA performance with the gain changing from -1 to $+1$. An input and output dynamic range of 300 mVpp was achieved, assuring wide linear range. This is illustrated over different control voltage settings showing bandwidth and gain relationship. The bandwidth of the proposed VGA is maintained over 7 GHz across the gain value, which is enough for 10 Gbps data transmission.

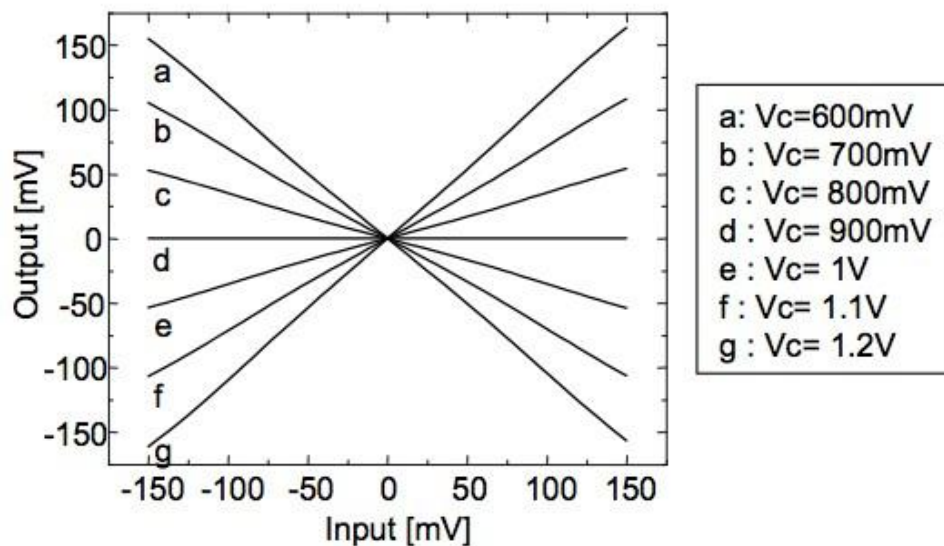


Figure 3-5. DC gain curve of the VGA cell showing dynamic range and linearity

The delay cell is implemented with series inductor (L) and shunt capacitor (C) as shown in Figure 3-6 [28, 29]. This artificial transmission line conducted by an LC ladder achieves the delay defined as $T_{delay} = \sqrt{L \cdot C}$. The lumped element analog LC delay line can work as a transmission line below the cutoff frequency; however, over this frequency, the input impedance of the lumped LC line will eventually be purely reactive. Input impedance is defined as $Z_{in} = \frac{j\omega L}{2} \left[1 \pm \sqrt{1 - \frac{4}{\omega^2 LC}} \right]$. The cut-off frequency is defined as $\omega_{cutoff} = \frac{2}{\sqrt{LC}}$ where the input impedance is purely reactive. The delay of such a cell is fairly constant over the wide band of the frequency. The passive delay cell can also provide fairly constant impedance characteristics over the frequency band of interest. From a simple calculation, we can verify that the lumped LC line has enough bandwidth to work as a delay line for a given equalizer structure. A 1.5 nH inductor is designed using an ASITIC (analysis and simulation of inductors and transformers in integrated circuits) simulator and then implemented by optimizing the line space and number of turns to increase the self-resonance frequency of the inductor by enhancing the Q factor.

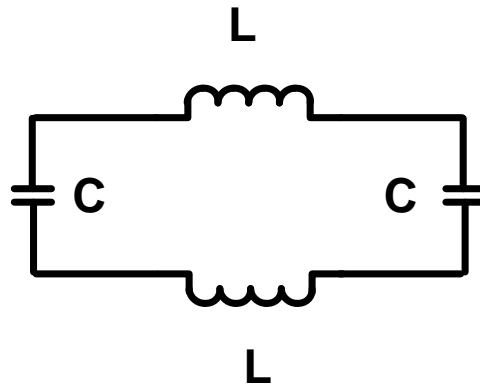


Figure 3-6. L-C delay line structure.

The FFE with a passive delay line structure is implemented in CMOS 0.18 μm and shown in Figure 3-7. From the figure, CMOS on-chip inductors occupy a large die area in the middle. The overall chip size is 1.09 mm by 1 mm including pad area. The total power dissipation for the passive delay line-based FFE is about 9 mW.

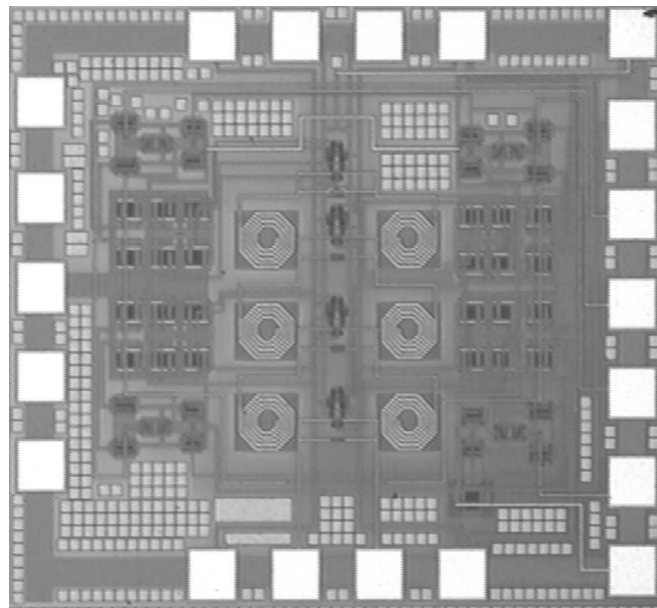
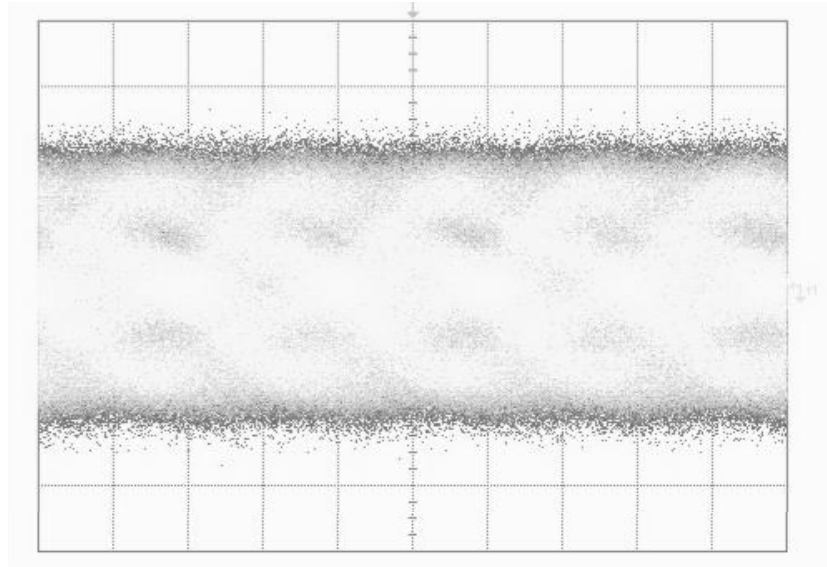
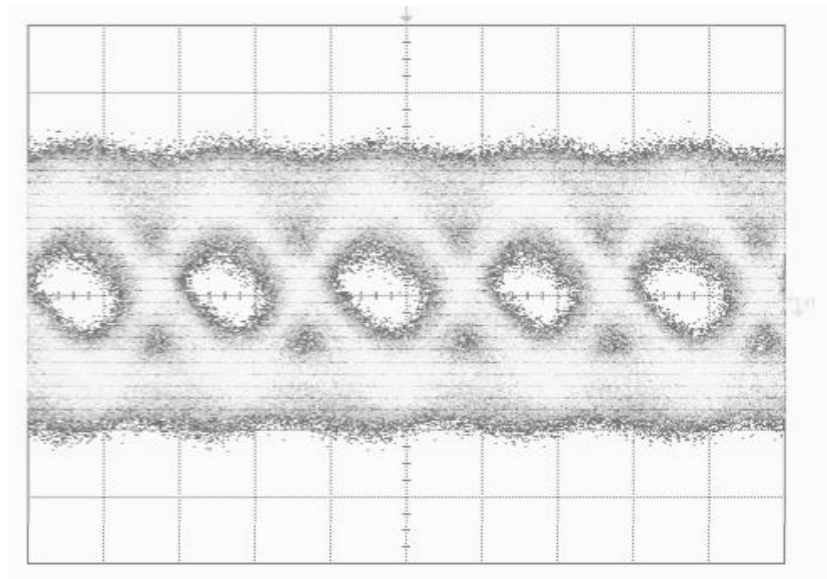


Figure 3-7. Die photograph of the passive FFE.

The 20-inch backplane channel with used to evaluate the performance of the FFE with a passive delay line. The 10 Gbps PRBS signal received from the output of the backplane is shown in Figure 3-8 a). The signal is severely impaired by ISI; therefore, the eye diagram is completely closed. Figure 3-8 b) shows the same eye diagram after the equalization. The majority of ISI is removed, where 10 Gbps data can be retrieved once the eye opening has been widened.



a)



b)

Figure 3-8. Measured performance of the FFE with a passive delay line with a 10 Gbps NRZ data input. a) before and b) after equalization.

B. Active delay line FFE

To avoid the large chip-area penalty associated with inductors and to reduce the vulnerability to process variations, we propose an active implementation of the delay line. However, the CMOS FFE with an active delay line lacks enough gain-bandwidth products to transmit the 10 Gbps signal. This prompts the use of a bandwidth extension method, inductive shunt-peaking, which is employed to create a peak in the frequency response of the delay-cell differential amplifier [30, 31]. An active inductor is implemented in this scheme to save on chip-area so that its effective value maximizes bandwidth and avoids time-domain ringing [32].

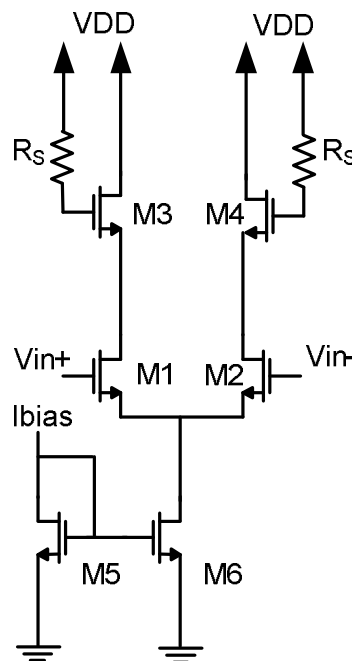


Figure 3-9. Schematic of the active unit delay cell.

For the unit delay cell of the CMOS FFE, shown in Figure 3-9,

$$Z_{in} = (1 + sC_{gs2}R_s) / (g_{m2} + sC_{gs2}) \quad (1)$$

R_s is the turn-on resistance ($r_{ds,on}$) of M1. The capacitance at the output node is given by

$$C_L = C_{gd3}(1 + H_0) + C_{db3} \quad (2)$$

where H_0 is the magnitude of the low-frequency gain.

Therefore, the voltage transfer function of the delay cell is

$$H(s) = \frac{g_{m3}(1 + sC_{gs2}R_s)}{g_{m2} + s(C_{gs2} + C_L) + s^2C_{gs2}C_LR_s} \quad (3)$$

with two poles and a left half plane zero.

Delay through active devices is a combination of the turn-on resistance and gate-source capacitance.

Hence, an estimate of the delay can be expressed as

$$\tau_d \approx R_s C_{gs2} - (C_{gs2} + C_L) / g_{m2} \quad (4)$$

The first term is usually dominant because the value of R_s and C_{gs2} is larger than that of the second term.

By varying the R_s , the zero location can be controlled. Figure 3-10 shows the bandwidth comparison between the active delay line composed of a differential pair with a passive resistor load and the one with active inductance loads [33]. The peaking adjacent to the dominant pole enhances the 3-dB bandwidth of the delay line by approximately 3.9 GHz compared with the bandwidth of the delay line with the passive resistor load. The simulation includes all the parasitic capacitance from both the multiplier cell and the adjacent delay cell.

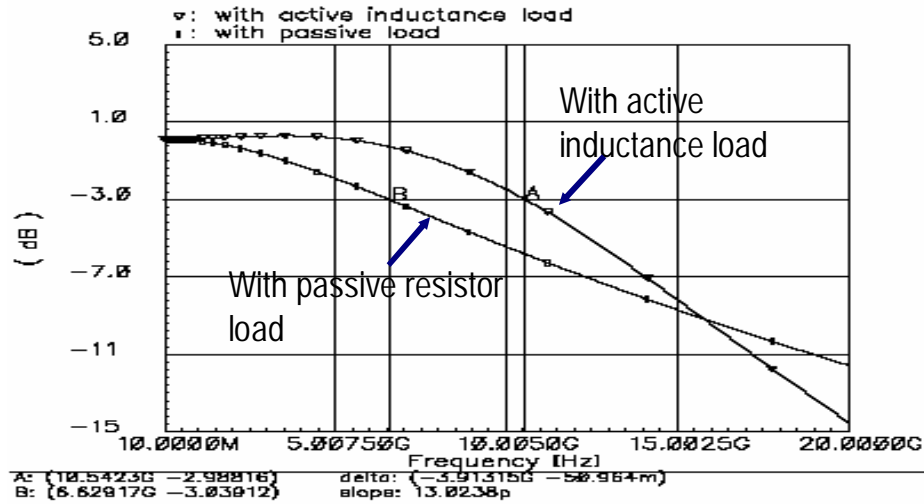


Figure 3-10. Bandwidth comparison of an active delay line with conventional passive load vs. an active delay with active inductance load.

For the initial active delay line implementation, two cascaded NMOS differential pairs are used each generating 33 ps ($T_s/3$) delay per unit delay cell. The effective inductance value, which is proportional to $R_s/(1/g_{m2})$, is optimized for 10 Gbps NRZ signal transmissions.

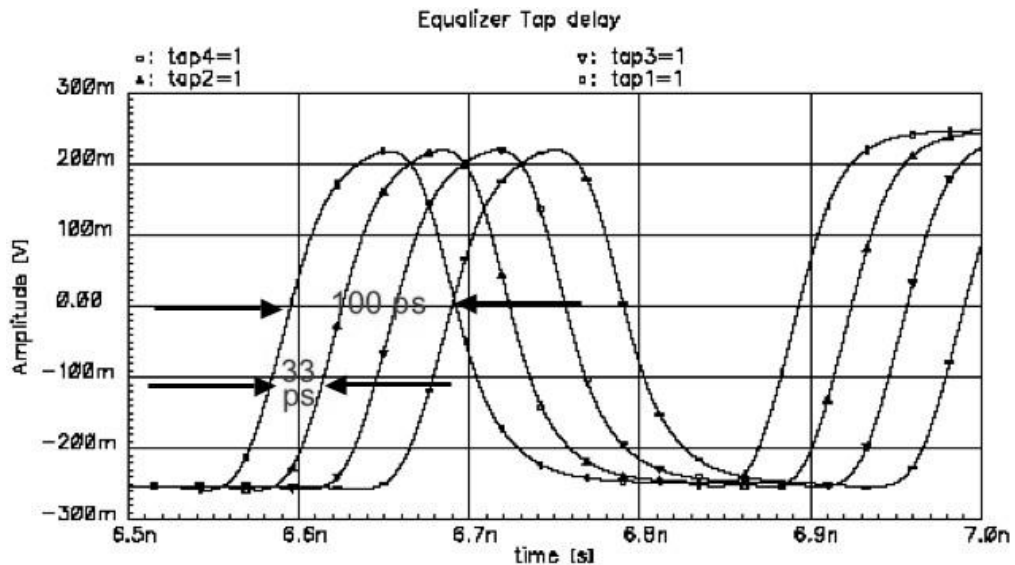


Figure 3-11. Active delay line performance in simulation

Figure 3-11 shows the simulation result for the designed active delay line. The measurement result shows accurate 33 ps tap delay spacing through the active delay line cells. No apparent slewing occurred on the measurement result, demonstrating enough bandwidth for high-speed data throughput.

Figure 3-12 shows the die photograph of the FFE with active delay line. The overall chip area is 1.15 mm by 0.89 mm including the pad area. The output buffer is included to match the impedance at the output. Total power dissipation of the active delay approach FFE is about 27 mW.

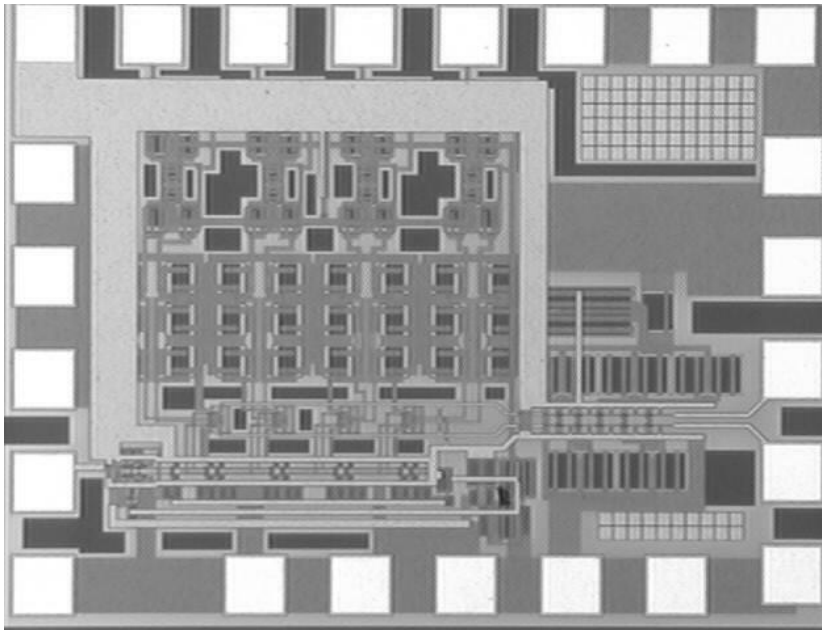
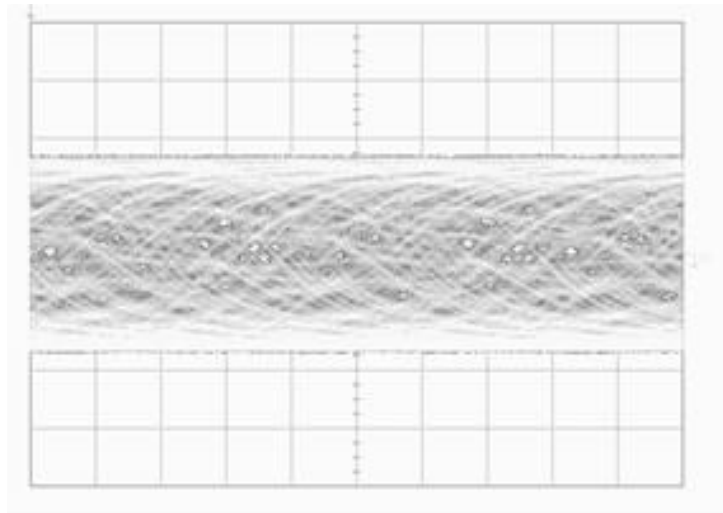
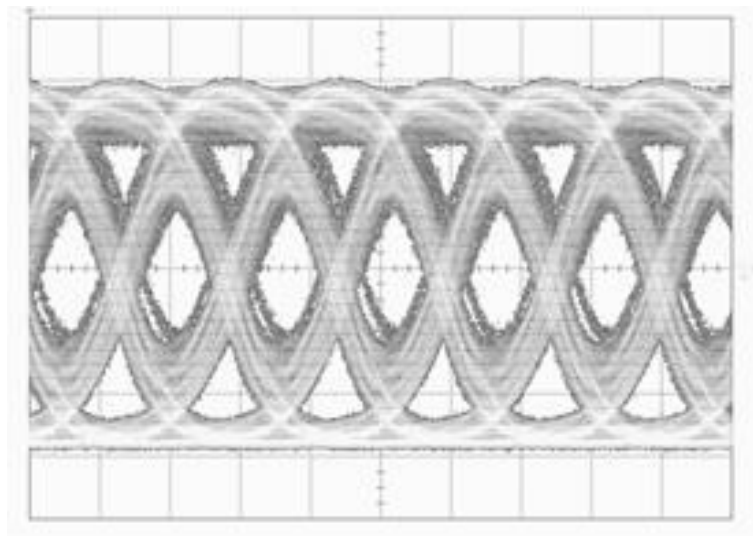


Figure 3-12. Die photograph of the active FFE.

Because active devices consume power, overall power consumption is higher in the active approach than in the passive approach. Without the output buffer, the equalizer core area is 50% smaller compared to that of the equalizer with passive delay line, while the power dissipation increases from 9 mW to 27 mW.



a)



b)

Figure 3-13. Measured performance of the FFE with an active delay line with a 10 Gbps NRZ data input after the equalization.

Measurement results of the FFE with the active delay line are shown in Figure 3-13, with an eye diagram of 10 Gbps after the equalization. Again, the majority of ISI is removed, providing an eye opening at 10 Gbps signal. Compared to the passive approach, this active approach results in a wider eye opening with smaller area.

Development of CMOS devices is driven primarily by shrinking the device dimensions, thinning the gate oxide, and lowering the supply voltages to achieve faster performance, increased density, and lower power consumption. The CMOS process is used mainly to implement digital logic. The smaller device lengths lower the parasitic components and increase f_T , but also necessitate complex designs, including halo implants, to minimize short-channel effects and to control punch-through. The CMOS 0.18 μm process, which was used in previous FFEs, featured a maximum f_T greater than 40 GHz, precision MIM capacitors, and five layers of metallization with a thick top metal layer. In comparison, the SiGe BiCMOS 0.25 μm technology offers maximum f_T greater than 65 GHz, MIM capacitors, and five metal layers also with a thick top metal. Another advantage of the BiCMOS process integrates high-performance heterojunction bipolar transistors (HBTs) with state-of-the-art field effect transistor (FET) devices. A detailed comparison of the two processes is explained below.

An intrinsic way to judge a given device as an amplifier is to look at its transconductance over the output transconductance (g_m/g_o), which is referred to as self gain. Transconductance is the ability of the device to source the current from the input voltage, and the output conductance tells how well that current is sourced with swings in the output voltage. Due to the exponential relationship between the output current and to the input voltage of the bipolar device, bipolar transconductance is much better than that of a FET, where the relationship is only quadric. Ultimately, the transconductance of the bipolar transistor is proportional to the I_c current of the device.

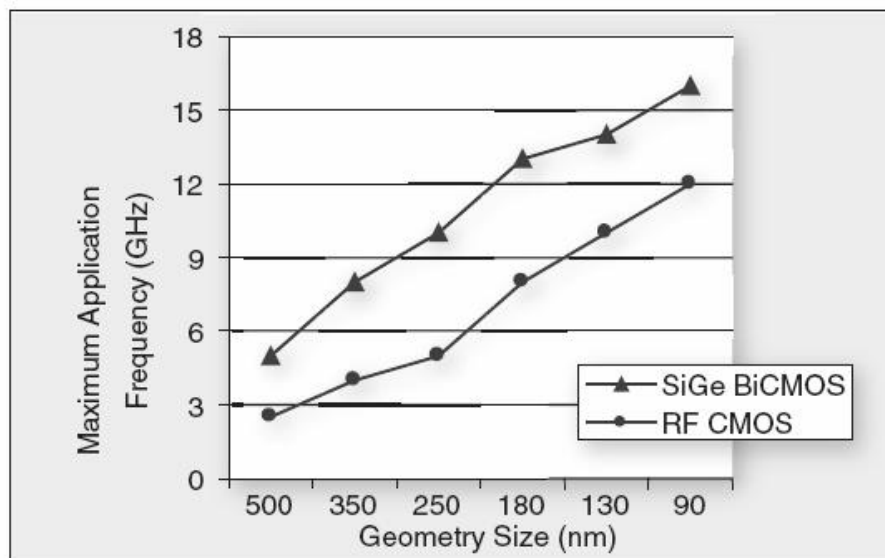
$$g_m (\text{BJT}) = q \cdot I_c / kT$$

whereas the transconductance of the FET is proportional only as the square root of its drain current,

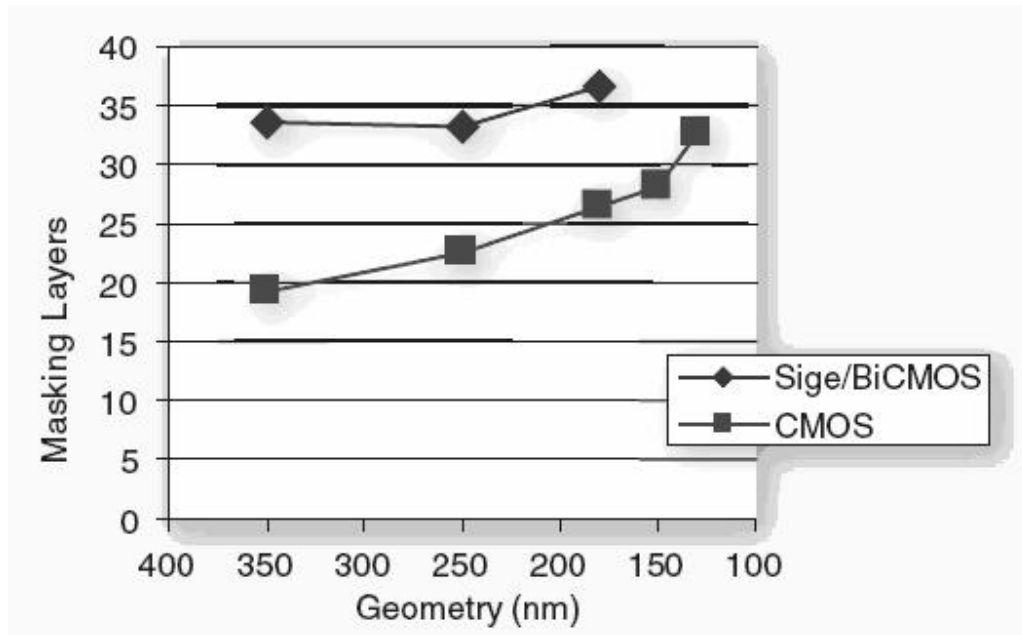
$$g_m (\text{FET}) = 2K \cdot \sqrt{I_D}$$

Roughly at its peak operating current, the BJT achieves about three times the transconductance, and thus three times the drive capability, of a FET.

The output characteristic of the device dictates the output conductance g_o . The flatter the current with the output voltage, the higher the output resistance and the smaller the output conductance $R_o = 1/g_o$. This characteristic can be easily improved by the device designer as BiCMOS processes offer quite a few control knobs. By using these to vary the concentration of Germanium, the designer can modify the electric field across the base and thus the carrier concentration, which improves the early voltage.



a)



b)

Figure 3-14. BiCMOS and CMOS process comparison of a) maximum application frequency by transistor size and b) number of layers vs geometry.

The most quoted figure of merits between different processes is the cutoff frequency (f_T) and the maximum frequency of oscillation (f_{MAX}). When process shrinks, lateral and vertical scaling lead to lower parasitic components and thus to faster speeds for the CMOS and BiCMOS devices. Especially in the BiCMOS process, modification of the doping SiGe layer is offered to increase in the electric field. This increase combined with the reduction in the graded base width, as well as the addition of carbon to decrease Boron out-diffusion, improves the base transit time, which further increases the device speed. The relation between the device speed f_T and the device transconductance can be described as

$$f_T(\text{BJT}) = g_m / (2\pi * (C_{BE\text{depletion}} + C_{BE\text{diffusion}} + C_{BC}))$$

$$f_T(\text{FET}) = g_m / (2\pi * (C_{BS} + C_{GD}))$$

All of these advances result in the overall reduction of the parasitics of the bipolar transistor, especially in the base, collector, and emitter resistances (R_B , R_C , and R_E) and in the total collector-base capacitance (C_{CB}). Coupled with the increased f_T , this reduction in parasitics is expected to lead to an increased f_{MAX} , which is the relationship between the two figures of f_T .

$$f_{MAX} (BJT) = \sqrt{f_T / (8\pi * C_{CB} R_B)}$$

$$f_{MAX} (FET) = f_T / 2 * \sqrt{(R_i + R_g + R_s) G_{ds} + 2\pi f_T R_G C_{GD}}$$

Maximum application frequency for CMOS and BiCMOS processes, which is typically $f_T/8$, is shown in Figure 3-14 a) for comparison.

Matching is one of the important factors in designing the analog circuit design. In the case of the bipolar devices, the matching of V_{bes} is determined by the doping profiles of the PN junctions across the emitter/base. With each technology improvement, these doping levels increase and the matching improves as well. In the CMOS devices, on the other hand, the equivalent is V_t matching. This depends more on the lateral dimensions of the devices, such as the L and W of the gate, as well as the doping levels in the active device. These are much less stable from device to device. Therefore, matching of the bipolar devices is better as compared to the matching of the CMOS devices.

The noise can be divided into two categories. One is low frequency noise ($1/f$ noise), and the other is high frequency noise such as noise figure (NF). NF is a measure of degradation of the signal to noise ratio (SNR), caused by components in the RF signal chain. $1/f$ noise is generated in distinctly different areas in bipolar and FET devices. In bipolar devices, the $1/f$ noise is mostly generated in the emitter/base junction. FET devices generate noise by the properties of Si/SiO₂ because they are surface conduction devices. This

means that the power of the $1/f$ noise is dictated by the quality of the PN junction and the oxide interface. Present-day HBT devices have a clean Si/SiGe interface, and their noise properties are significantly better than that of CMOS devices. Moreover, generation-to-generation scaling in FET devices moves oxide interfaces even closer to the active channel, resulting in increasing the $1/f$ noise.

As in high frequency noise, NF is the quantity that compares the SNR at the output of the amplifier to the SNR at the input of the device. NF is the ability of the amplifier to amplify the signal without adding any noise to it. NF depends on the intrinsic properties of the device, emitter resistance (R_E) and base resistance (R_B), internal capacitances and transconductance. Basically the relationship is that the lower the parasitics (R_E , R_B , C_{CB}) and the higher the transconductance, the lower the NF will be. The SiGe bipolar devices feature several intrinsic properties that make them attractive for low-noise circuits. The addition of Germanium makes it possible to heavily dope the base of the device without the increased hole injection into the emitter. Heavier doping decreases the base resistance and therefore lowers the thermal noise of the base. A second source of high frequency noise in the BJT devices is the shot noise generated by the carriers crossing the PN junctions. The shot noise in the base depends on the magnitude of the base current injected into the emitter. Due to the nature of the heterojunction, the injection of holes from the base into the emitter is significantly reduced for a given I_c current. This minimizes the noise contribution on the device input. Furthermore, the high amplification of the bipolar devices contributes to the high gain. This high gain allows an input signal to be amplified to higher levels compared input signals which have been increased by the addition of thermal and shot noises. This high gain reduces the impact of these noises on the output SNR and improves the NF.

CMOS devices also exhibit improvement in NF with shrinking. Lower effective gate lengths increase the device's transconductance and amplification ability. Also, heavier doping of the source and

drain regions improves the R_S and R_D which degrades the SNR. Despite these advantages in CMOS, the SiGe HBT device most likely provides better performance due to its much higher transconductance.

Another technical consideration is to have a whole set of different chips integrated into one chip solution. Usually, CMOS devices are used for integrating digital logic functions with high-speed bipolar analog circuits. This allows fully integrated system-on-chip products, with the CMOS performing the lower-frequency baseband signal processing. With a CMOS-only process, the analog functions need to be done with the FET transistors. This will degrade the gain, matching, and noise. However FET transistors are ideal in cases like ADCs since CMOS devices draw no current at the gate and, therefore, do not disturb the input signal.

There has been significant development made in CMOS and BiCMOS process scaling. CMOS gate lengths have shrunk, gate oxide thickness has decreased, and power supply voltage has dropped. These improvements have provided increased die density, faster transistor speed and lower power consumption. However, scaled CMOS in analog circuits does not always guarantee a benefit other than speed. Because of the lower supply voltage, it can not hold many stacks of transistors while biasing in the saturation region. Also, the thin oxide layer contributes to the excess noise and current leakage. BiCMOS, on the other hand, achieves faster speeds without these drawbacks.

Even though the cost of process scaling can be significant during the introduction of technology, these costs decrease quickly as the technology matures. Part of this initial cost increase is attributed to mask costs. As shown in Fig. 3-14 b), at a given node, CMOS nodes typically require fewer masking steps than does the BiCMOS process. This generally results in lower wafer cost and faster manufacturing cycle times. However, as the number of masking steps increases with CMOS scaling, the cost advantage offered by CMOS begins to erode as geometries decrease. Additionally, CMOS scaling may not proportionally scale

with the die. The fact that die shrinks in a mixed-signal system-on-chip when CMOS scales down greatly depends on how much of the analog area is dominated by passive components.

All fabricated ICs are measured by wafer-level probing methods to avoid package-induced parasitic. As propagation delay through the tapped-filter is a parameter that decides the FFE performance, it is useful to note that the delay varies as the RC-product at several circuit nodes in the signal path. This phenomenon is impacted by junction capacitances for HBTs and by the fact that overlap/field-oxide capacitances for MOSFETs differ. Because of the higher f_T and gain of the BiCMOS process, the design for the proposed research is implemented in BiCMOS to accommodate the higher data rate.

3-3. CIRCUIT DETAILS OF THE BICMOS ACTIVE DELAY FFE

According to the system simulation in the previous section, the equalizer with four taps was decided to be the optimum solution for the backplane channel. It consists of the four-tap active delay line ($T_s/3$), four Gilbert variable gain cells (C1-C4), and buffer stages between the delay line and the gain cells as shown in Figure 3-15. An additional fourth delay stage is included for the matching. The buffer stage is necessary because, unlike MOS devices, BJT devices exhibits low input impedance. The signal path is fully differential. Each tap gain and gain polarity is controlled using external DC voltages. The output of each tap is summed up at the passive load. The tap spacing for 10 Gbps signal width is 33 ps, which is 1/3 of 100 ps.

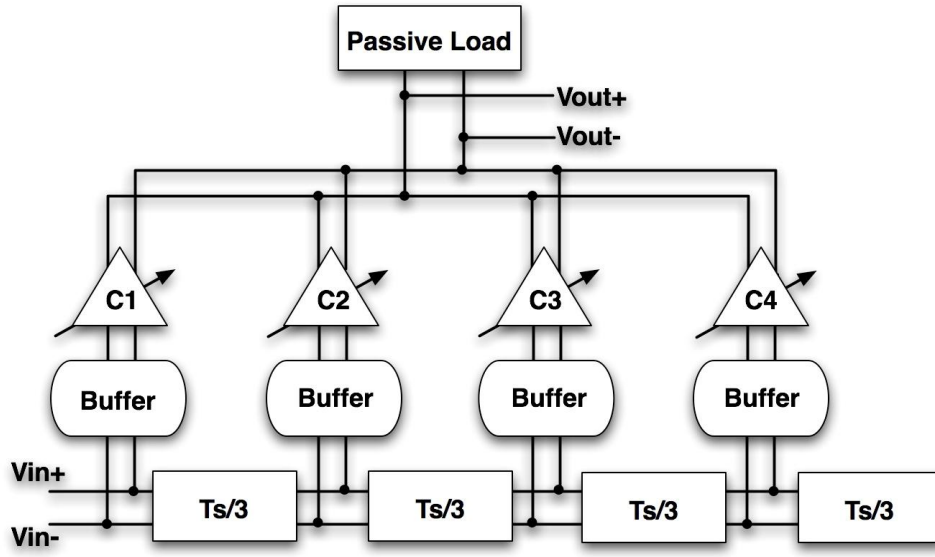


Figure 3-15. BiCMOS FFE system block.

A. Active Delay Line

The active delay line implementation is shown in Figure 3-16. While the passive delay line consumes more area, the active delay line is more compact without requiring excessive power consumption. Two more benefits of the active delay approach are that it does not introduce DC voltage drops across each stage and that the overall bandwidth is not drastically degraded by additional delay stages. After investigating different approaches for analog delay cells, we found that the key trade-off is between the achievable delay and small-signal bandwidth.

All the delay cells are cascaded, shown in Figure 3-16. One delay cell has two differential pairs. The last delay cell is added just for matching purposes. A side effect of cascading delay cells is the reduction of the gain as the signal goes through the delay line. To compensate for this loss of the gain, small gain buffers

are used in a series with the delay cells. The delay of the cell is set by the $gm - C$ product. The $gm - C$ product is also a function of the bias current. Our target delay amount is 33 ps because one third of the 10 Gbps signal width is 33 ps. Through the careful selection of transistor size, a delay amount of 33 ps is achieved with enough bandwidth for the above 10 Gbps applications [34].

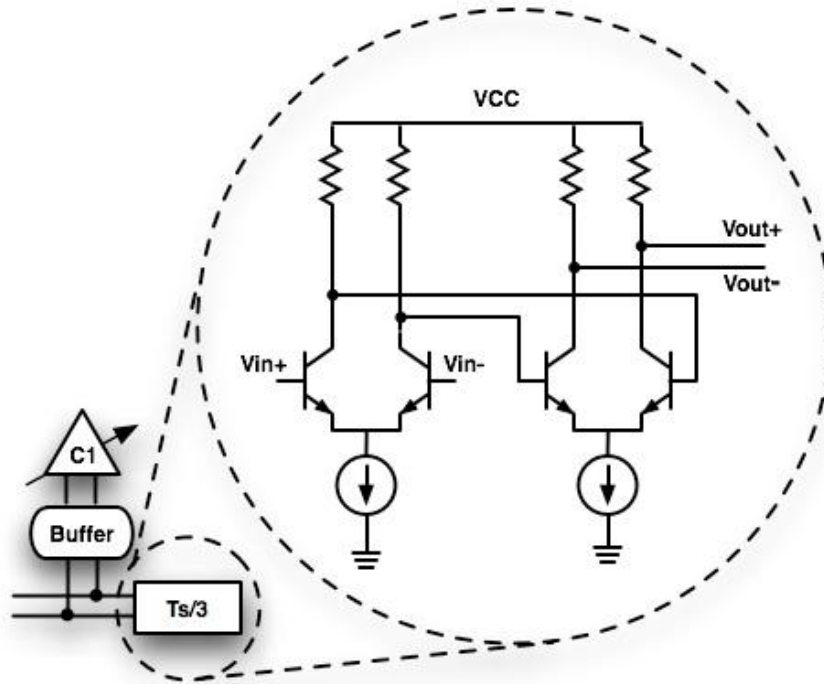


Figure 3-16. Active delay line implementation.

B. VGA

The Gilbert cell, shown in Figure 3-17, is used as a gain stage for various tap gains. A folded current control block such as the one used in CMOS technology in the preliminary research is not necessary for the BiCMOS circuit as a 3.3 V supply affords sufficient headroom. Also, in the case of the BiCMOS FFE, all differential pairs in the Gilbert cells are implemented with HBTs so as not to impair the wide-band 10 Gbps signal, and the devices have f_T characteristics of about 57 GHz. The tail current mirror and reference are,

however, designed with MOSFET devices for linear operation. The tail current of a differential pair controls the tap gain, while two control signals determine the polarity of the gain. The input signal is fed into Q1 and Q2. The upper differential pairs decide the sign of the gain depending on which pair is activated. The Gilbert cell acts as a voltage-to-current converter so that the filter response can be combined at the tap at the summing node. A differential pair is buffered from the signal through the delay line to reduce the loading effect. The signal path from the input is designed with BJT transistors to accommodate the wider bandwidth signal. Bias current for this design is 7 mA.

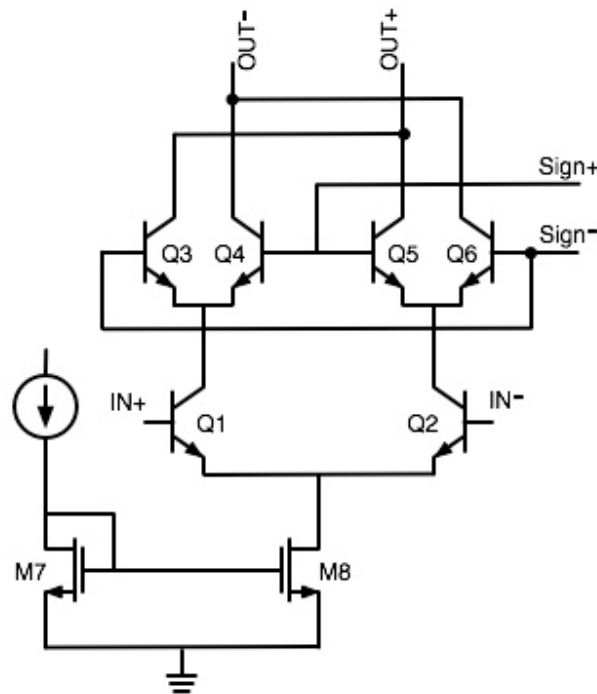


Figure 3-17. Schematic of the VGA.

C. Simulation Results of BiCMOS Active Delay FFE

To verify the circuit operation, it is essential to show the gain variations with input control voltages. The eye diagrams in Figure 3-18 show the gain variations. The amplitude of the eye diagram varies

according to different input control voltages. It varies from 40 mV to 100 mV, and the polarity of the gain can be changed with external control voltage.

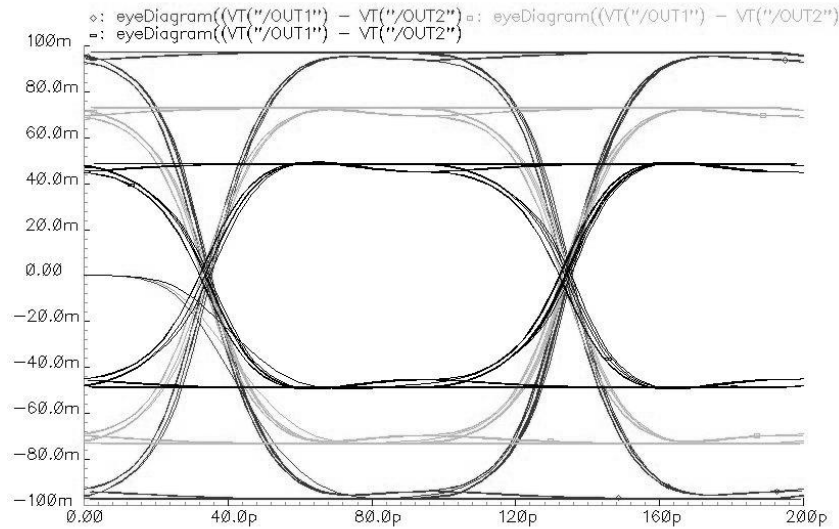


Figure 3-18. Performance of the VGA.

The active delay line performance is also presented. For proper system operation, achieving 33 ps delay per tap is very important. Exact tap spacing requires compensation in the frequency domain. The result of the exact delay is shown in Figure 3-19. These pulse signals are drawn by turning only one tap on and then plotting the output. The first eye diagram is drawn with tap number one turned on, and other three taps turned off. The second eye diagram is drawn with tap number two on and other three taps off. It shows approximately 33 ps between signals as shown in the distance between markers. The other two signals (number three and four taps) each show the same delay.

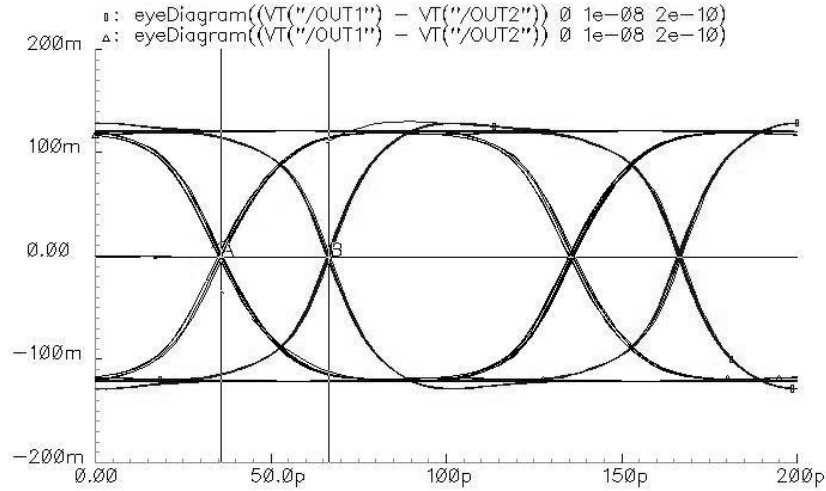


Figure 3-19. Performance of the active delay line.

D. Measurement Results of BiCMOS Active Delay FFE

The micrograph of the BiCMOS FFE is shown in Figure 3-20. The circuit occupies an area of 1mm x 1mm, including pads, and is fabricated in a 0.25 μm BiCMOS process technology. The actual core is significantly smaller than 1 mm x 1 mm because all the DC pads and paths to the pads occupy most of the area. The core block is only about 0.25 mm x 0.1 mm. Differential inputs and outputs are located on the left side and the right side of the circuit respectively. The bias and the control signal pads are located along the top and the bottom sides of the circuit. Other pads are connected to the ground. BiCMOS transistors are used in the signal path through the chip for more bandwidth. Metal five is used for the most of the signal paths to reduce the resistivity. For example, a metal one is used in the ground path for better isolation from the signal path. The inputs and outputs are probed to reduce the noise along with DC control voltages. The power supply is 3.3 V, and the current for a nominal tap setting operation is 14 mA.

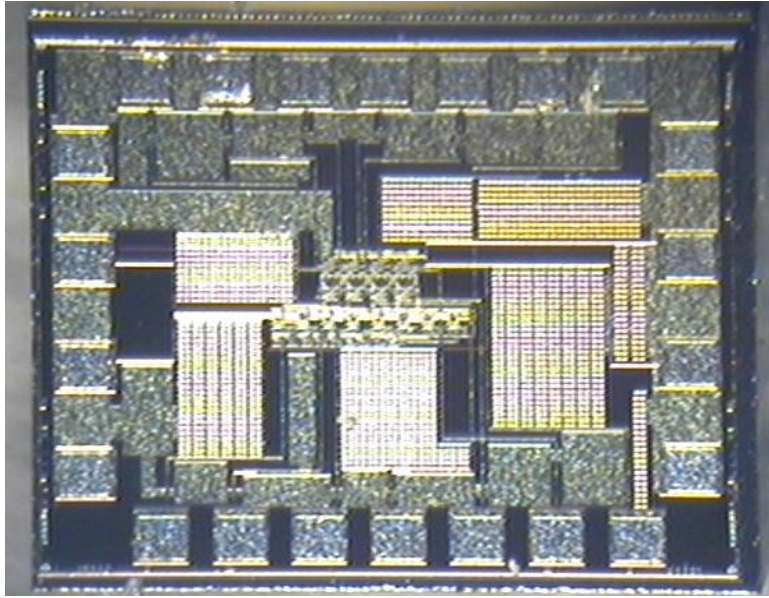


Figure 3-20. Die photograph of the BiCMOS active FFE.

The Gilbert cell multipliers can have bi-polarity gain according to the control voltage. A 10 Gbps chain of pulses is input into each FFE, and the tap-delay is measured in order to verify the delay cell performance. The results of this measurement are shown in Figure 3-21, where each curve represents the pulse waveform when only one tap is turned on. The curves are superimposed synchronously with a common reference input. These plots show that the BiCMOS delay units yield 35.2 ps delay per tap. The departure of the BiCMOS FFE from the ideal result is only minor and may not be reliably attributed to physical quantities, though the relatively loose tolerance of the load resistors is a factor.

Figure 3-22 shows the experiment setup for the measurement of the FFE IC performances. First, the basic functions of the 4-tap FIR filter, such as the delay line performance, are measured. Then, the equalization performances are measured for the 10 Gbps NRZ signal over 20 in the FR-4 backplane channel.

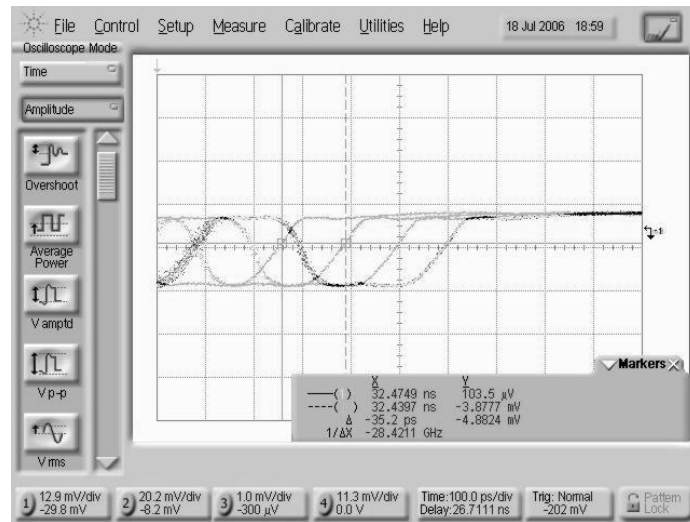


Figure 3-21. BiCMOS FFE delay line measurements.

The setup consists of a Bit-Error Rate Tester (BERT), DC sources, a Digital Sampling Oscilloscope (DSO), and an FR-4 backplane PCB board with two daughter cards. The BERT generates the differential-ended transmit signal at the pre-determined data speed, 10 Gbps in this experiment. This input signal is connected to the FFE IC for the basic filter functions, i.e. tap delay and gain characteristics. Then, the FFE output signal is provided to the DSO for verification of the filter functions. Meanwhile, the transmit signal is connected to the daughter card for the equalization performance measurement. The corresponding channel output signals are obtained from the daughter card at the other end of the backplane board. These channel output signals are fed into the FFE IC for the equalization. The DC sources provide the tap gain control voltages from 400 mV to 1.4 V for a linear gain between -1 and +1. Finally, the equalizer output signal is connected to the DSO, and the corresponding waveform and eye-diagram are observed. This FFE IC is manipulated on the probe station.

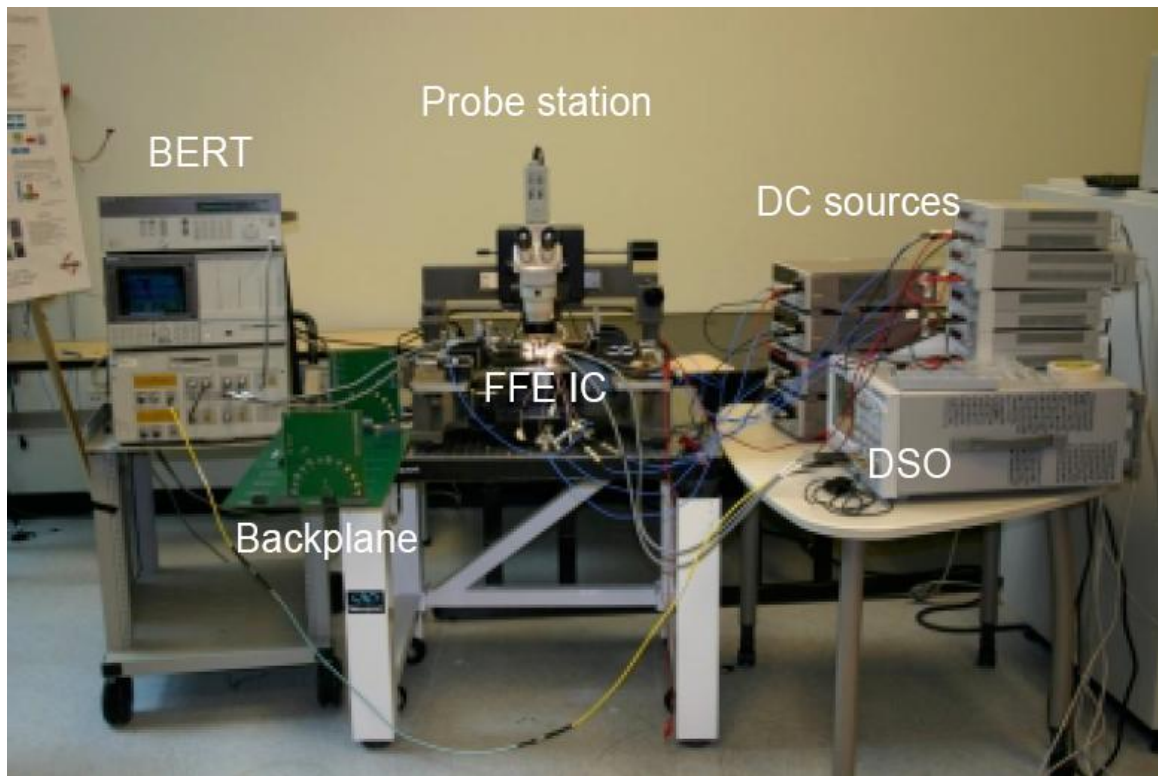
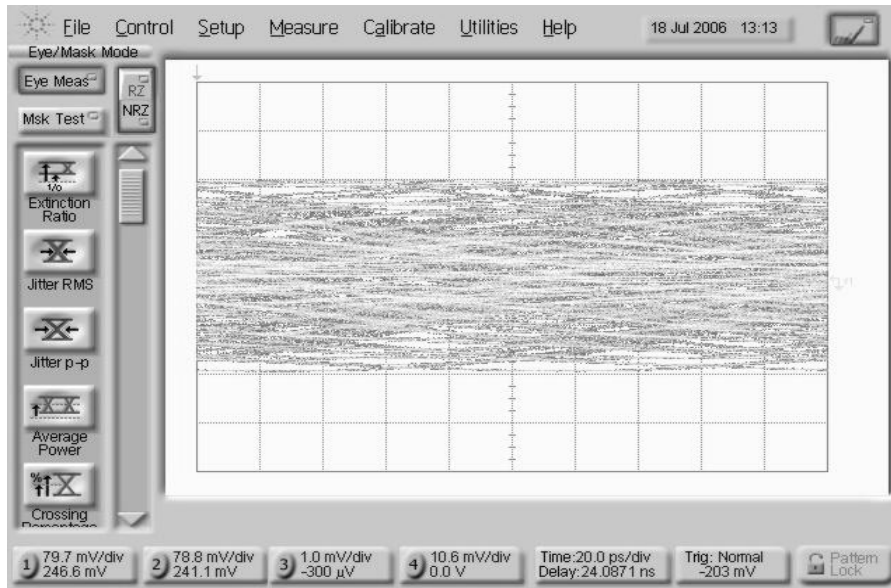
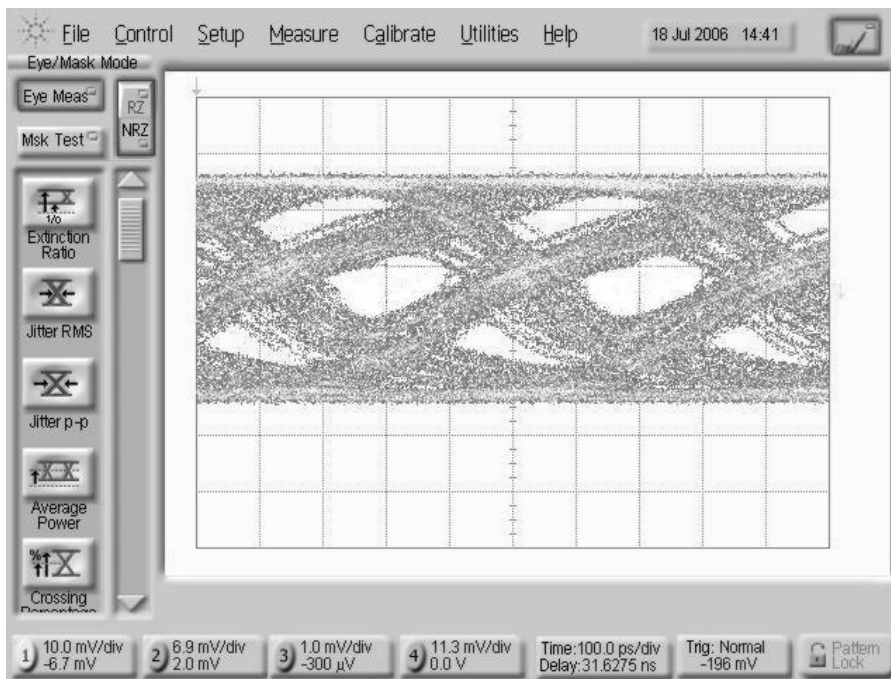


Figure 3-22. Experiment setup for measurement of the fabricated CMOS FFE IC performance.

The eye-diagram showing the direct received signal without equalization is plotted in Figure 3-23 a) along with plots showing the signal after equalization by either FFE. Before equalization, the received signal is so affected by ISI as to render the data irrecoverable. This is represented by the closed eye of Figure 3-23 a). After equalization, the BiCMOS FFE succeeds in opening the eye-diagram, allowing the data to be recovered as shown in Figure 3-23 b).



a)



b)

Figure 3-23. Eye diagram a) before equalization b) after equalization.

CHAPTER IV.

EQUALIZATION FOR GPON CHANNELS

4-1. SYSTEM SIMULATION FOR 1.25 GBPS GPON LINK

A. Fabry-Perot Laser

One of the critical parts of GPON links is the laser. The distributed feedback (DFB) laser and electro-absorption modulated laser (EML) are stable solutions [35]; however, they are expensive to build. For a more cost-effective system [36], the Fabry-Perot (FP) laser is a good candidate because it is manufactured by a high yield process which does not require equipment-intensive grating and overgrowth steps [37]. The structure of the FP laser is shown in Figure 4-1. An FP laser consists of an electrically pumped PIN junction as a gain medium. It consists of two specially designed slabs of semiconductor

material on top of each other. Another material is placed in between them, forming what is known as the “laser cavity.” Electric current flows through the device from the top to the bottom, and the emission of light occurs in the laser cavity.

The FP lasers, however, exhibit multiple spectral modes, as shown in Figure 4-2, whereas GPON systems use single mode fiber (SMF) with a single spacial mode characteristic. As a result, the relative power throughout the various spectral modes can fluctuate significantly even though the total optical output power of the FP laser is fairly constant. This phenomenon is known as mode partition noise (MPN) [38].

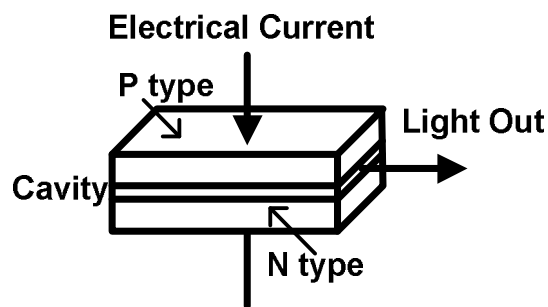


Figure 4-1. Fabry-Perot laser structure.

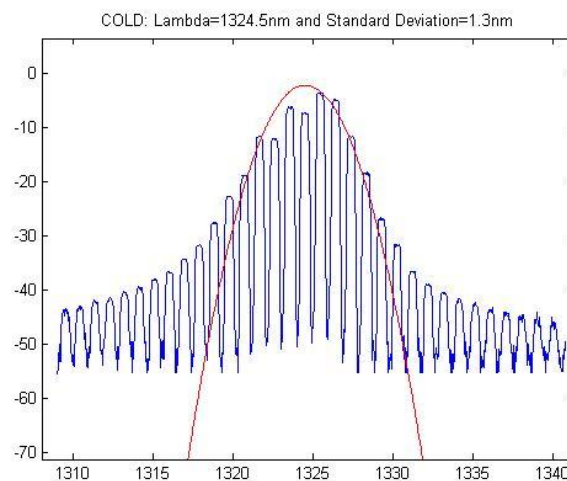


Figure 4-2. Measured spectrum of the Fabry-Perot laser.

This MPN, in conjunction with chromatic dispersion (CD), results in ISI on the receiver side, significantly degrading the system performance at the corners. This dissertation suggests using an FP laser in the upstream link and correcting for ISI resulting from the FP laser and single mode fiber in order to have a cost effective system. This work does not address the downstream path, which uses a DFB laser, and therefore does not suffer from ISI related problems. Previous approaches to compensate for ISI mostly use optical components, which are bulky and expensive [39, 40]. This work suggests using the EDC to address the problem in the electrical domain [41, 42].

A preliminary analysis of the GPON links from the ONU to the OLT was necessary to better understand the link to be equalized. The downstream path, which uses a DFB laser with a good signal quality due to the absence of MPN, has good transmission characteristics. However, the upstream path (utilizing the FP laser) has limiting characteristics that need to be discussed. Here we develop an analytical model, taking into account the main impairments that impact the link performance: thermal and shot noise in the receiver, CD in the fiber and MPN from the laser. The bit error ratio (BER) data extracted from this analytical model is compared with the actual measured BER data to verify the accuracy of the model.

B. GPON Upstream Signal Path

The GPON upstream signal path is composed of an FP laser in a triplexer on the ONU side, 0 to 20 km of SMF, and a receiver on the OLT side. A triplexer is a bi-directional transceiver, which converts an electrical signal into an optical signal. It contains a Fabry-Perot laser diode with a monitor photodiode, a high-bandwidth avalanche photodiode and a trans-impedance amplifier (TIA) for a digital receiver, an analog photodiode for a video channel with low noise and high linearity, and a matching network built directly on the chip. This upstream path transmits the signal through the FP laser.

C. Upstream Link Model

The laser output spectrum is typically modeled by a Gaussian distribution around a center wavelength with a standard deviation [43]. Figure 4-2 shows the measured spectrum (blue) and the associated Gaussian fit (red). The spectral width of the laser can be derived from the standard deviation of the Gaussian distribution using the full width at half maximum method (FWHM).

$$FWHM = \sigma \cdot 2\sqrt{2\ln(2)} \quad (1)$$

In order to test the system in different situations, the laser is temperature tuned to change the center wavelength. This accounts for the dispersion-induced penalties on the system. At room temperature, the laser properties are measured to have a center wavelength of 1324.5 nm and a spectral width of 3.0 nm. As the temperature is increased, the spectral width remains constant but the spectrum shifts to a higher wavelength. The Tuned Temperature (TT) is defined as the temperature where the center wavelength of the FP laser is 1328.5 nm, the longest experimental wavelength value.

In this thermal noise, for limited upstream link, the BER for a back-to-back configuration can be derived as a function of the average input optical power P_{IN_AVG} using

$$BER = \frac{1}{2} \operatorname{erfc} \left(\frac{1}{\sqrt{2}} \frac{MRP_{IN_AVG}}{\sigma_R} \right) \quad (2)$$

where R is the responsivity, M is the average avalanche multiplication gain of the avalanche photodiode (APD) receiver, and σ_R is the receiver noise. The noise in the receiver can be derived from the thermal noise defined as

$$\sigma_{Thermal}^2 = \frac{4k_B T}{R} F_n BW \quad (3)$$

where T is the temperature, F_n is the noise figure of the following low noise amplifier, and BW is the electrical bandwidth of the receiver. The receiver noise is also derived from the shot noise of the photodiode, defined as

$$\sigma_{Shot}^2 = 2eM^2F_A(M)RP_{IN_AVG}BW \quad (4)$$

In (4), e is the elementary charge and $F_A(M)$ is the excess noise factor of the APD.

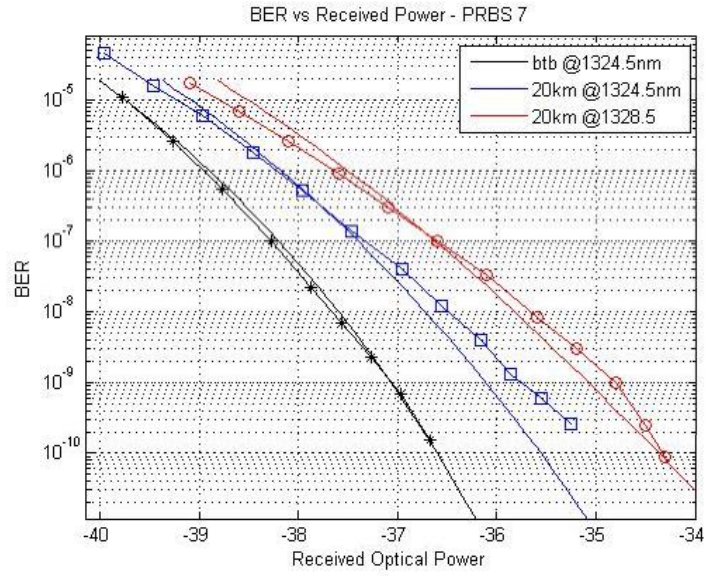


Figure 4-3. Comparison between simulated and measured BER.

The receiver can be practically characterized by the BER back-to-back curve. With an electrical bandwidth of 640 MHz, a value that is slightly higher than half the bit rate, the computed back-to-back BER is

displayed in Figure 4-3 as a solid black curve, and the experimental data points as black crosses. The back-to-back simulated results correlate with the actual measurements.

Based on this receiver characterization, the two critical power penalties of the system (MPN and CD) are analyzed and included into the model in order to simulate the 20 km BER performances (Figure 4-3) and evaluate the weight of each effect. A detailed explanation of these impairments will be covered in the next section.

D. Chromatic Dispersion and Mode Partition Noise

Group velocity dispersion in single mode fiber leads to the broadening of the optical pulse [44]. If a significant part of the pulse energy spreads beyond the allocated bit slot, it will affect the previous and/or next bit, resulting in ISI after the electrical conversion [45]. Moreover, the pulse energy within the bit slot is reduced when the optical pulse broadens, which requires more average energy to maintain the system performance, resulting in a power penalty due to dispersion. The optical pulse can be modeled as a Gaussian pulse, and an analysis of its broadening properties leads to the following expression of the dispersion induced the power penalty [46]:

$$\delta_d = -5 \log_{10} \left[1 - (4BLD\sigma_\lambda)^2 \right] \quad (5)$$

where B is the bit rate, D is the chromatic dispersion, and L is the distance. Since dispersion theoretically is a linear process, this power penalty can be compensated by an EDC.

The other impairment, MPN, is typically found in Fabry-Perot lasers, where the output optical spectrum has different longitudinal modes. It can be assumed that the total power is constant even if the amplitude of the peak is constantly varying. When the signal propagates through the fiber and is affected by group velocity dispersion, each mode is delayed by different amounts.

The varying amount of power in each mode submitted to chromatic dispersion leads to an additional noise. This was theoretically investigated by K. Ogawa [47], in whose model the noise to signal ratio after the transmission is expressed by

$$\sigma_{pc}^2 = \frac{1}{2}(\pi B)^4 \left[A_1^4 \sigma_{\lambda}^4 + 48 A_2^4 \sigma_{\lambda}^8 + 42 A_1^2 A_2^2 \sigma_{\lambda}^6 \right] \quad (6)$$

Where

$$A_1 = \frac{2\pi c}{\lambda_0^2} L * \left. \frac{d^2 \beta}{d\Omega} \right|_{\Omega_0}, \quad (7)$$

$$A_2 = \left(\frac{2\pi c}{\lambda_0^2} \right)^2 L * \left. \frac{d^3 \beta}{d^3 \Omega} \right|_{\Omega_0} \quad (8)$$

and the propagation constant $\beta(\Omega)$ is derived with respect to $\Omega = 2\pi c / \lambda$ at $\Omega_0 = 2\pi c / \lambda_0$.

Then, the power penalty resulting from MPN is given by

$$\delta_{MPN} = 5 \log \left(\frac{1}{1 - Q^2 (k \sigma_{pc})^4} \right) \quad (9)$$

where we have introduced a coefficient, k . This k coefficient was used by Ogawa and Vodhanel [48] to take into account the fact that the amplitude of each spectral mode does not vary from very small to maximum peak, but fluctuates by only 100*k percent, or 70 percent in our model, of total optical power [49]. MPN results in a non-deterministic component of inter-symbol interference [50].

The accuracy of the model is evaluated by comparing the computed BER to the measured BER of the link in different configurations [51]. Three significant configurations are tested. Figure 4-3 is the summary of the simulated BER compared to the experimental data for each of the three configurations. The black line in the graph is the back-to-back BER data. The blue curve displays the BER data with 20 km

SMF at the center wavelength of 1324.5 nm. Finally, the red plot shows the 20 km fiber data at the 1328.5 nm wavelength.

The simulated curves in Figure 4-3 are consistent with the experimental data measured from the upstream link and allow us to evaluate the amount of power penalty caused by CD and MPN. Power penalties (P_p) for the BER of 10^{-9} for the two link configurations are summarized in Table I.

TABLE I
POWER PENALTY COMPARISON AND ANALYSIS FOR DIFFERENT WAVELENGTHS

Link	20 km at 1324.5 nm	20 km at 1329.5 nm
P_p dispersion	0.38 dB	0.69 dB
P_p MPN	0.84 dB	2.49 dB

σ_{MPN} is also proportional to σ_L , which is the rms value of the laser spectral width. The formula which links two variables is expressed as

$$\sigma_{MPN} = \frac{k}{\sqrt{2}}(1 - \exp(-(\pi BCL\sigma_L)^2)) \quad (10)$$

where B is the bit rate, D is the chromatic dispersion, and L is the distance. This rms deviation of the centroid data gives a clear picture of the laser beam pointing stability. In order for 1 dB penalty to be allowed in the system, the laser spectral width needs to be lower than 1.5 nm, which is a very stringent number.

The goal of this design of the EDC is to improve the power penalty of the system using an EDC. To evaluate the EDC's performance in the GPON link, an overall GPON system with the EDC transfer function is simulated. If MPN gets worse, the laser spectral width will increase because the effect of the laser modes power fluctuation is equivalent to an increase in average spectral width. Using this model with the formulas above, we achieve the results of the power penalty that are depicted in Figure 4-4. The blue line represents the outcome based on the Agrawal Theory, and it closely matches the analytic approach using the formulas above, which are represented as the pink graph. System simulation with an EDC is performed with 3 tap and 5 tap EDCs with different delays. The 3 tap penalty is shown as the red line, the 5 tap as the green line in Figure 4-4. The result shows that the reduction in MPN due to the EDC allows an increase in laser spectral width up to 3 nm.

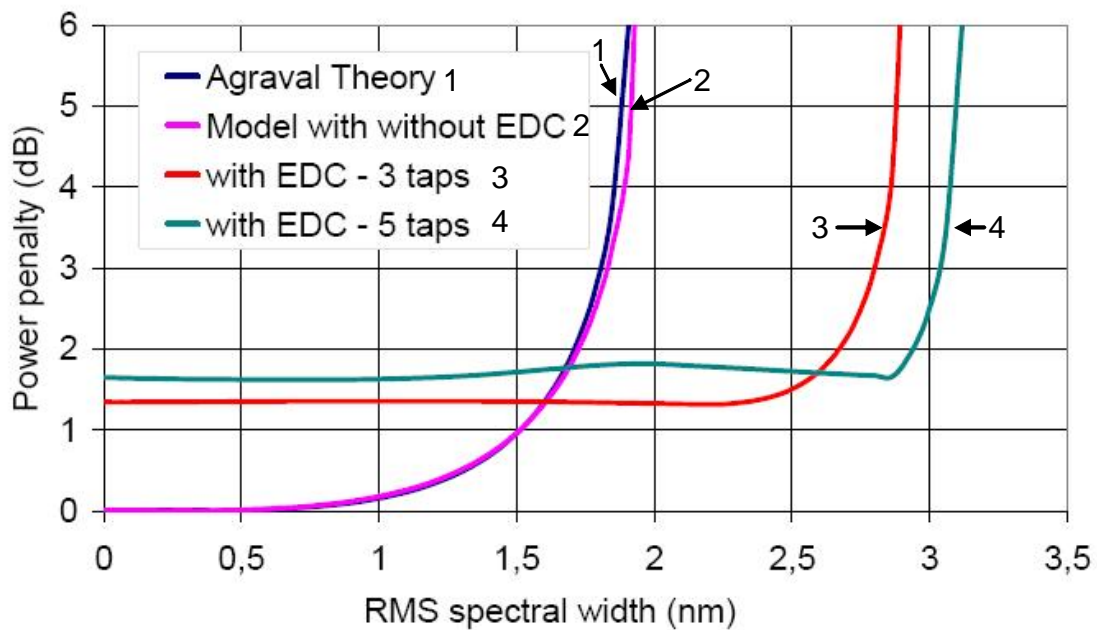


Figure 4-4. GPON link simulation with the 3 and 5 tap EDC.

4-2. ELECTRONIC DISPERSION COMPENSATOR FOR GPON LINK

We chose an FFE structure with four taps and tap spacing of τ over three at 1.25 Gbps for the EDC based on the preliminary research, as shown Figure 4-5. The system simulation, shown in Figure 4-4, predicts that four taps with a spacing of τ over three is sufficient to compensate for dispersions up to 20 km and to reduce the power penalty of the overall system. Adding more taps to the system results in only marginal improvement of ISI at the cost of power consumption, bandwidth, and size.

The FFE structure consists of a single-to-differential converter, the variable gain amplifiers (VGA) (C1-4), delay cells (τ), and a limiting amplifier (LA), as represented in Figure 4-5.

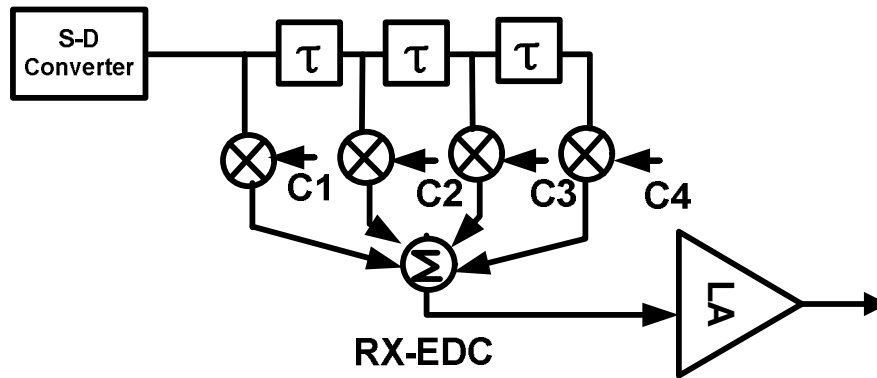


Figure 4-5. Functional diagram of the EDC.

GPON links have various channel characteristics that are dependent on the fiber length and zero dispersion wave-lengths. EDCs can be placed either on the ONU side or the OLT side. Placing an EDC on the ONU side has the advantage that the link could be compensating for a specific fiber dispersion value since fiber dispersion changes very little with temperature. However, this structure would require 32 or more transmitter-side EDCs in the ONU and would increase the cost of customer side equipment. When an

EDC is placed in the OLT, the cost of the EDC is shared by 32 users, resulting in a more cost effective solution. A single-to-differential converter is placed at the EDC input in order to convert a single-ended signal into a differential signal [52].

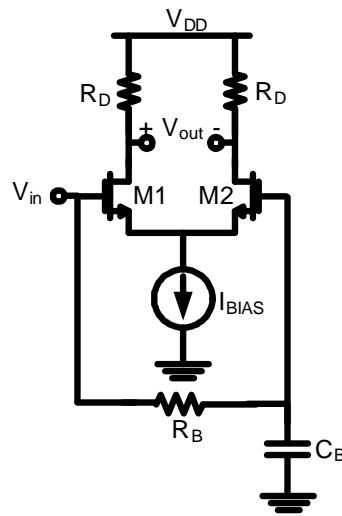


Figure 4-6. Schematic of the single-to-differential converter.

Optical systems are usually single-ended, whereas the integrated analog circuits used in high-frequency applications are fully differential in order to make them able to reject common-mode noise and achieve high voltage swings [53]. Therefore, a stage that converts a single-ended signal into a differential signal needs to be added.

The single-to-differential conversion circuit composed of a differential pair with one of its inputs grounded is shown in Figure 4-6 [54]. The unused input of the differential pair is the gate of M2, whose DC bias voltage is supplied through a low-pass filter comprised of R_B and C_B . The input signal propagates to the $+V_{OUT}$ node through a path where M1 operates as a common-source stage, generating an inverted signal, and to the $-V_{OUT}$ node through a path where M1 and M2 operate as a cascade of a source follower and

common-gate stage, generating a non-inverting signal. The gain of this circuit is set by the ratio of the transconductance of M1 and M2, which can be adjusted by varying their aspect ratio.

Delay cells can be implemented using active or passive components. For the optical link, the delay cells are implemented with NMOS differential pairs, as shown in Figure 4-7, to improve space efficiency as compared to a passive delay approach. The propagation delay of the active delay is generated by the R-C's transient characteristic, i.e. resistance of the load and intrinsic capacitance of the differential amplifier pair cells.

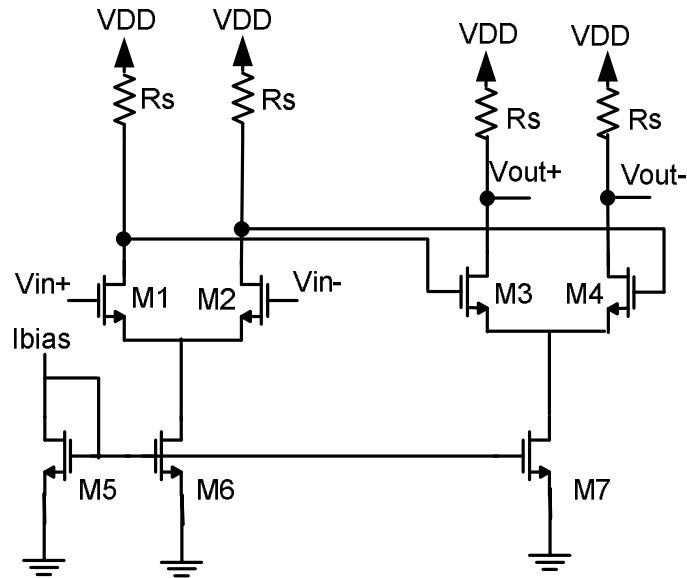


Figure 4-7. Schematic of active delay cell.

The overall voltage gain of the differential pair in unit delay cell is

$$A_v = g_m \cdot (Z_{in} // C_L)$$

where the corresponding C_L and Z_{in} values can be calculated as follows:

$$C_L = C_{gd} (1 + A_v) + C_{db}$$

and

$$Z_{in} = \frac{sC_{gs} \cdot R_s + 1}{sC_{gs} + g_m}$$

The two poles are at

$$-\frac{1}{2} \left(\frac{C_{gs} + C_L}{C_{gs} C_L R_s} \right) \pm \frac{1}{2} \sqrt{\left(\frac{1}{C_L R_s} + \frac{1}{C_{gs} R_s} \right)^2 - \frac{4g_m}{C_{gs} C_L R_s}}$$

and the zero is at

$$\frac{1}{R_s C_{gs2}}$$

By varying the R_s , (R_s is turn on resistance of the load transistor), the zero location can be controlled. Another benefit of the active delay is that it is immune to process variations because of its lack of passive devices. The passive delay approach is an attractive solution for power saving but achieving 267 ps delay with L-C passive components requires large amount of space.

The VGA is a Gilbert-multiplier type amplifier which has positive and negative gain. Currents out of VGAs are summed at a passive node. The schematic of the VGA is shown in Figure 4-8.

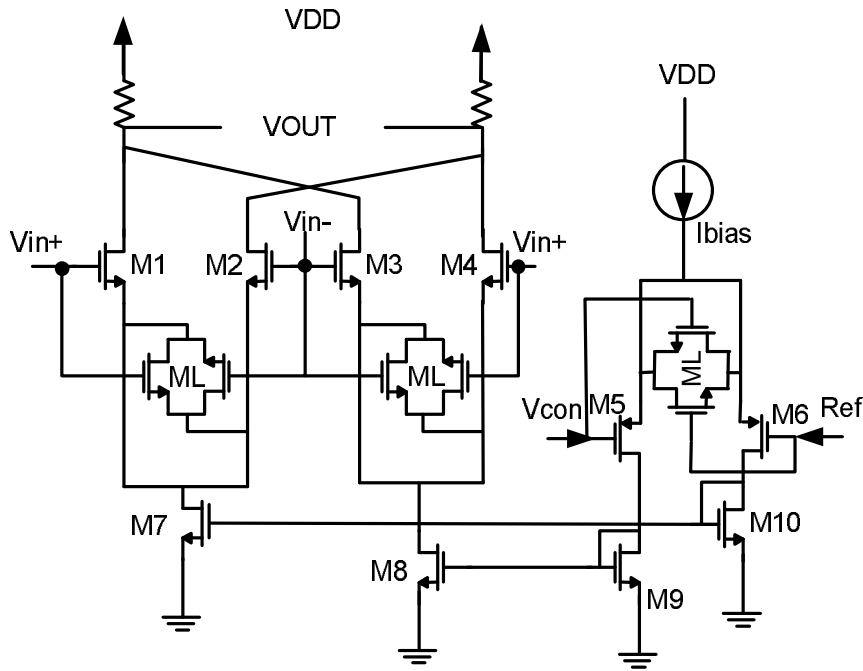


Figure 4-8. Schematic of the VGA.

In addition, both linearity and voltage headroom are enhanced by applying an active degeneration scheme between divided common source pairs. The ML transistor pairs represent such active degeneration, with M7, M8, M9, and M10 being the divided current sources. The gain control block also includes a degeneration circuit (ML) for linear gain control. Transistor sizes are adjusted from the backplane FFE version because its bandwidth requirement is relaxed.

The limiting amplifier is two cascaded differential pairs and is matched to 50 ohm, as shown in Figure 4-9. Because the FFE structure needs to provide enough voltage swing at the output, a limiting amplifier is required. Instead of using an identical gain cell for two stages, each stage is designed differently with the first stage designed for gain and the second stage designed for matching. The output stage also increases the slew rate by allowing a large-signal current swing.

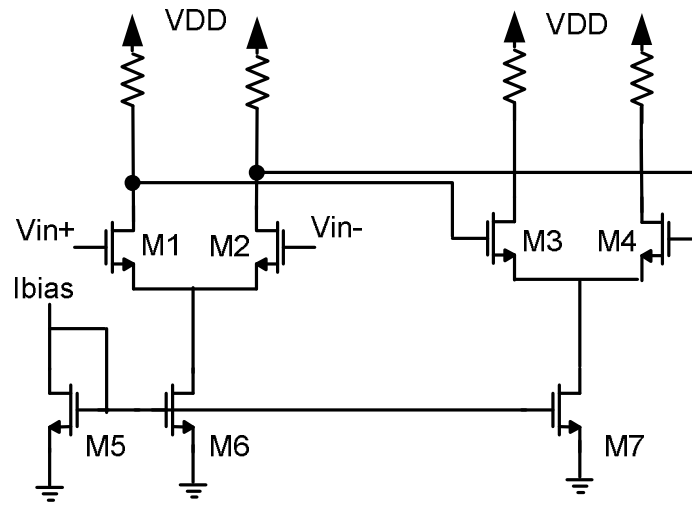


Figure 4-9. Schematic of the limiting amplifier.

The input voltage swing to the buffer is large enough compared to the offset input voltage, so no offset compensation is needed. The 3 dB bandwidth of the output buffer is about 7 GHz, which does not degrade the signal integrity at the output of the EDC.

4-3. MEASUREMENT RESULTS OF THE ELECTRONIC DISPERSION COMPENSATOR FOR THE GPON LINK

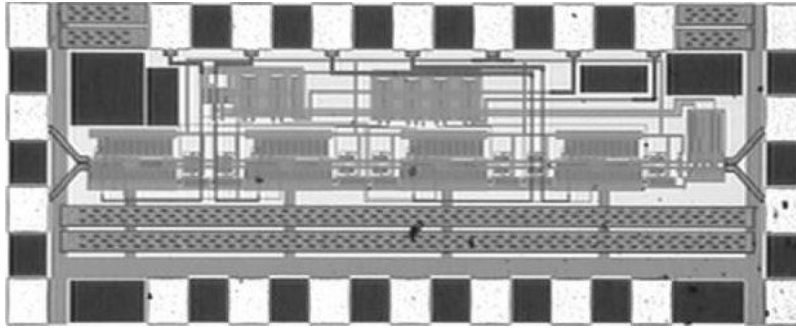


Fig 4-10. Micrograph of the EDC for a GPON system.

To measure the performance of the EDC, the GPON experimental link is set up. The FP laser in the ONU receives 1.25 Gbps electrical signal generated by the BERT, which is then converted into the optical signal. This optical signal is transmitted through 0 to 20 km SMF and is converted to an electrical signal using a photo diode. The triplexer converts an input electrical signal into an optical signal. This optical signal is then transmitted through 0~20 km single mode fiber. The optical receiver consists of a PIN/TIA photo detector and a low-noise amplifier (LNA). The electrical signal is fed into the EDC, and the output of the EDC is monitored with a digital sampling oscilloscope. The zero dispersion wavelength of SMF used in the experiments is 1310 nm. The EDC is implemented in TSMC 0.18 μm CMOS technology. Actual size of the EDC including pads is 1.7 mm by 0.75 mm. The die microphotograph is shown in Figure 4-10. The supply power is 1.8 V, and the power consumption is 54 mW. The measurement set-up for the GPON experimental link is shown in Figure 4-11. A 1.25 Gbps pseudo-random bit signal (PRBS) with a word length of 2^7-1 is transmitted. Figure 4-12 shows the bit patterns before and after compensation. The bit pattern before compensation shows uneven zero and one signal levels, which is an indicator of ISI. After applying the EDC, the appropriate compensation the signal levels are improved at the output of the EDC [55]. The performance of the EDC is also evaluated in terms of error ratio. The EDC is tested with a PRBS signal for experimental purposes. The EDC will work even in a burst mode for the GPON application because it is transparent to modulation.

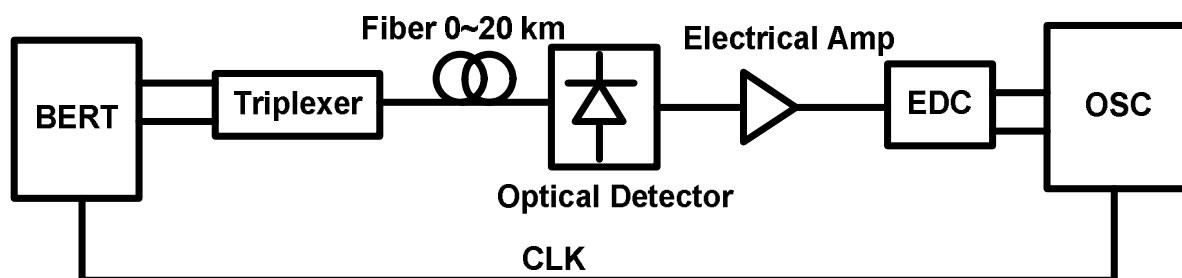


Figure 4-11. A GPON link for measurement of the EDC.

The concept of transparent EDC is introduced and is used as the reference for the GPON link performance, which is affected by the EDC measurement set-up. In this configuration, the first tap of the EDC is set to a constant coefficient, a gain of one, and the three others are set to zero. Figure 4-13 compares the BER performance of the EDC in the transparent configuration with that of the optimized configuration, where the tap coefficients were tuned to compensate for dispersion.

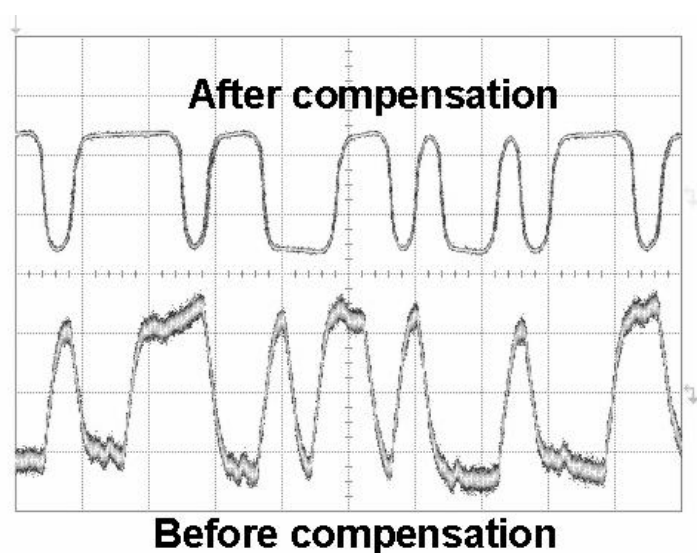


Figure 4-12. Bit pattern before and after compensation.

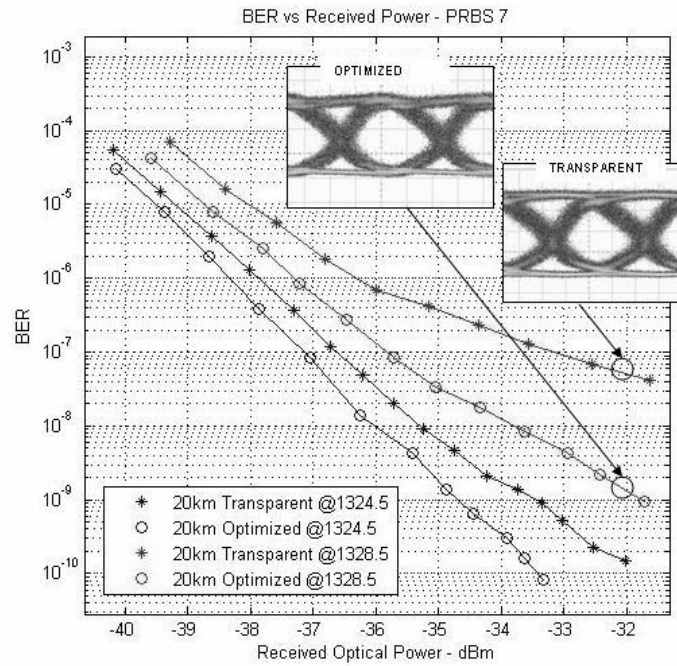


Figure 4-13. Comparison of BER between the transparent and the optimized EDC.

For the laser at both 1324 nm and 1328 nm, compensation leads to a shift of the BER curve to a lower received power, compensating for the power penalty due to dispersion. The dispersion compensation provided by the EDC enables the system to overcome ISI penalties and get an access to lower BER needed for communication purposes.

CHAPTER V.

BALANCED FEED-FORWARD EQUALIZERS

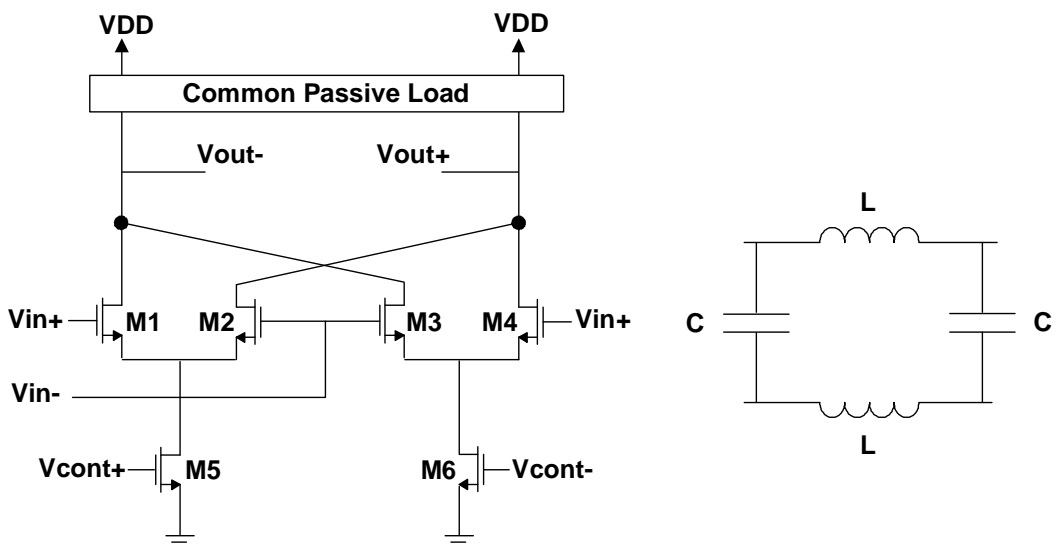
5-1. OVERVIEW OF PASSIVE EQUALIZERS

Previously mentioned in chapter 3, tapped delay line-based FFEs can use either passive or active delay cells. Although to the best of our knowledge, there is no specific data available on the optimal number of taps, in general, a greater number of taps in the FFE provides better compensation for longer channels [56]. However, with more than a few taps, implementing a good on-chip layout by using passive delay cells becomes very difficult. The inductors used in passive delay cells occupy a large area and cause difficulty in signal routing. The signal and bias lines become long, creating significant loss and parasitic cross coupling in the circuit. The bandwidth is also severely degraded due to the high amount of parasitic capacitive loading on the signal path. Moreover, it is very challenging to maintain linearity in gain and constant group delay over large bandwidth since the long lines have large parasitic components that can introduce spurious poles and zeroes in the characteristic response. The solution to these problems lies in the implementation of structures that can reduce the parasitic effects in FFEs with a large number of passive delay cells.

This chapter highlights the effect of using different configurations on FFE performance through the study of two functionally equivalent but differently structured FFEs. In section 4-2, an overview of the two test structures is given, along with a short description of the building blocks used. Section 4-3 provides results of the performance of the two structures with two fabricated layouts.

5-2. TWO EQUALIZER STRUCTURES

The current FFE structures under investigation are designed with 3 dB target bandwidth specifications of 3 GHz and a gain of 0 dB for GPON and coherent detection applications [57, 58]. Both FFE designs are based on a tapped delay line Finite Impulse Response (FIR) filter structure. Each structure has nine taps with a uniform tap spacing of 80 ps. The two structures differ from each other only in that the delay cells in one of the structures are all on the input side, while those of the other structure are evenly distributed between the input and the output. For ease of description henceforth, the two structures will be referred to as the unbalanced (delay cells only at the input) and the balanced (delay cells evenly distributed between input and output) structure.



a)

b)

Figure 5-1. VGA schematic a) and the passive delay cell structure b).

The main building blocks of the FFE are Variable Gain Amplifiers (VGA) and delay cells, which are shown in Figure 5-1. The VGA block is the same structure as that used in the previous approach. It is implemented with a Gilbert cell-based structure for linearity of operation. The current steering block is degenerated with active devices to achieve high linear performance [59]. The delay cell is implemented with a series inductor (L) and a shunt capacitor (C). This artificial transmission line conducted by the LC ladder achieves the delay, defined as $\tau = \sqrt{LC}$. Cut-off frequency is defined as $\omega = 2/\sqrt{LC}$, where the input impedance is purely reactive. The delay of such a cell is fairly constant over a wide band of frequency. The passive delay cell can also provide fairly constant impedance characteristics over the frequency band of interest. Previous chapters have shown active delay cells as an alternate technique for delay line implementation. Active delay cells provide loss and die size benefits at the cost of higher power consumption. In this chapter, however, the focus is on the passive delay cell-based FFEs only,

A. Unbalanced Structure

The unbalanced structure is a direct-form implementation of the FFE transfer function. The output of the FFE is derived by the summation of the output of different delay taps multiplied by appropriate weight as shown in Figure 5-2. The nine taps are obtained from a long chain of eight unit delay cells, each providing a delay of 80ps. The input delay line is terminated in a matched impedance to suppress multiple reflections.

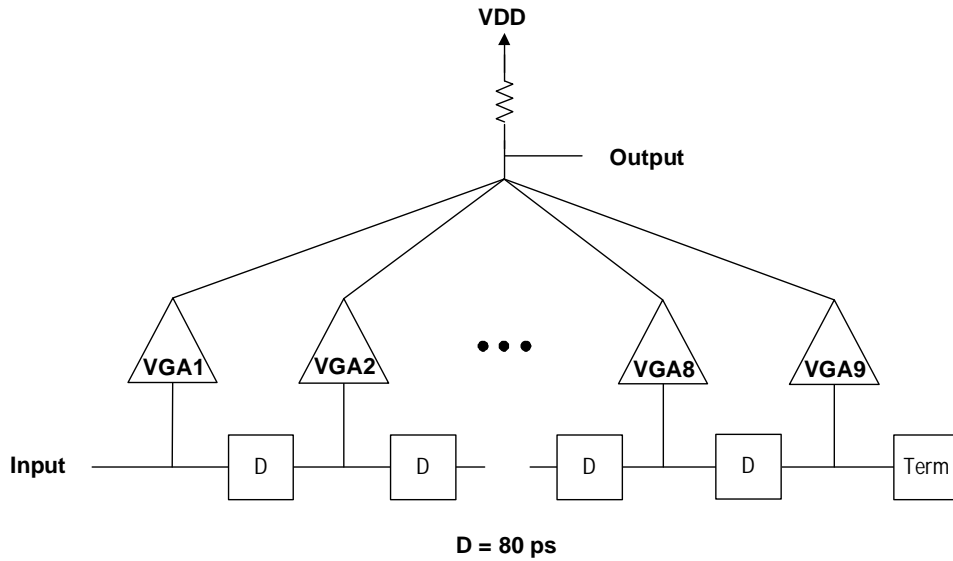


Figure 5-2. Unbalanced FFE functional block diagram.

The delay cells, however, consume a large area, so the signal routing from the VGA outputs to the summing node becomes very difficult. The long and unequal signal lines from the VGA outputs to the summing node can cause a significant amount of random phase error over different processes and temperature corners in the output of each tap and thus can degrade the overall accuracy of equalization. This problem is at least partially addressed by folding the unbalanced structure at a point between the fourth and the fifth taps to reduce the length of the signal paths from the VGA outputs to the summing node. Due to the high capacitive loading from the drain capacitances of all nine VGAs at a single node, the bandwidth is degraded. Moreover, the signal in the input delay line suffers considerable loss due to the high series resistance of the inductor in the passive delay cells. This can cause a large amount of deviation in the effective tap gains from the actual set value. Such errors can be minimized by taking into account the delay line characteristics when calculating the tap coefficients and by introducing booster amplifiers to compensate for the losses in the long delay line. Lastly, the bias current consumed by all nine VGAs flows across the summing node, causing a significant DC voltage drop and reducing

the voltage headroom. The voltage headroom in this structure is limited by a voltage drop across the summing node plus two stacks of transistors in the VGA cell.

B. Balanced Structure

The balanced structure is implemented as a traveling wave structure. A total of sixteen differential delay cells of 40 ps each are distributed evenly between the input and the output paths as shown in Figure 5-3. The signal is tapped from the nine delay points and added at the output with the VGA. The summation is achieved at different points in the output delay line, which consists of eight delay cells of 40 ps each. Both the input and output delay cells are terminated with matching load to suppress multiple reflections [60]. The signal at the output node is the linear superposition of the signal components arriving through different paths at the output. The overall delay in each path is the sum of the corresponding delays in the input and the output paths.

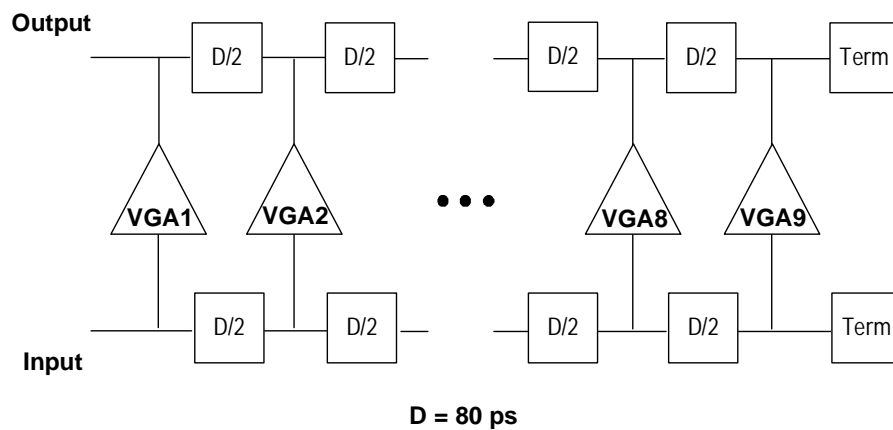


Figure 5-3. Balanced FFE functional block diagram.

Since the outputs are not summed at any single point, this structure can be implemented with shorter and equal length signal paths from the VGA outputs to the summing nodes. This structure reduces the parasitic components associated with the signal and bias lines, leading to a considerable improvement in bandwidth and voltage headroom. The distributed summing also reduces the effective overall capacitance at the output node, leading to an increased bandwidth [61]. Also, because there are now multiple summing nodes at the output delay line, the voltage headroom is consumed by only two stacks of transistors in the VGA. This means that each VGA can utilize more current for better overall gain of the FFE without the headroom issue.

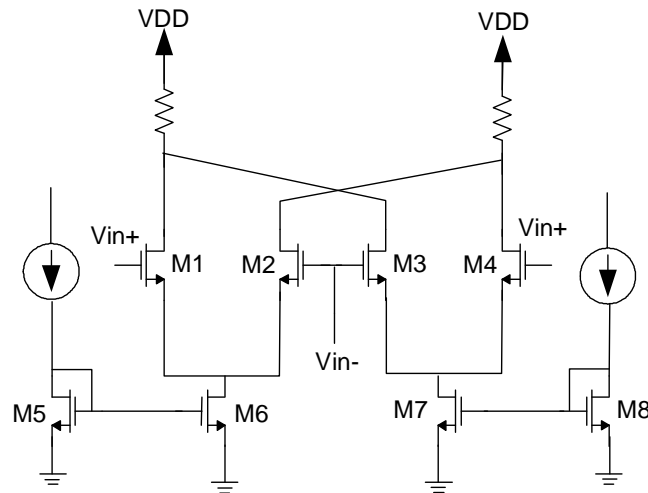


Figure 5-4. VGA core of the balanced delay FFE.

VGAs in the balanced delay FFE take advantage of the extended voltage headroom to achieve higher gain. As shown in Figure 5-4, VGAs are cross-coupled devices with two legs that control the sign of the VGA gain. We need two controls over the VGA; the first one is analog gain control and another one is sign control. For better controllability, by using a sense amplifier, we can merge these two controls into one. A sense amplifier circuit is used to sense and refresh the value of a bit stored in a memory cell of a dynamic random access memory (DRAM) integrated circuit. There are many versions of sense amplifiers used in

memory chips. The one that we use in the design is called a cross-coupled sense amplifier demonstrated in Figure 5-4.

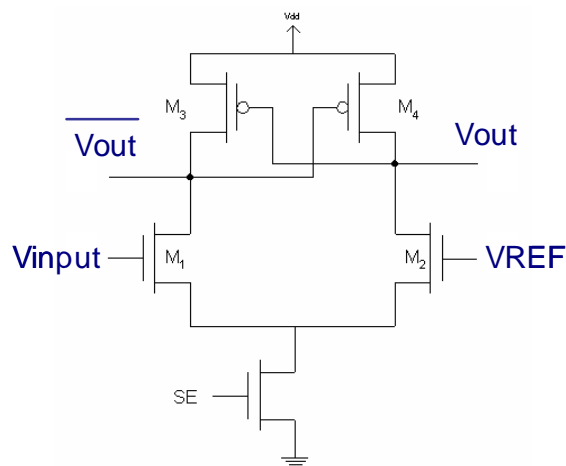


Figure 5-5. Schematic of the sense amplifier.

A sense amplifier here is incorporated with a VGA to activate each leg of a VGA bias circuit. As shown in Figure 5-5, if VCTRL is larger than VREF, then a transmission gate on the IA side is activated to have a non-inverting gain at the VGA output. If VCTRL is smaller than VREF, the other transmission gate on the IB side is activated to have an inverting gain at the VGA output. For linearity gain of the VGA, current mirror circuits are sized differently for both legs.

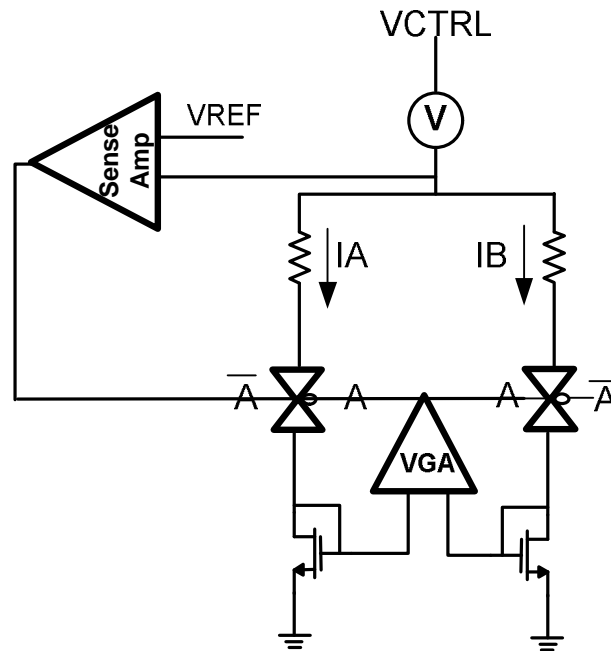


Figure 5-6. Schematic of the VGA of the balanced delay FFE with a sense amplifier.

Simulation results are shown in Figure 5-7. When V_{REF} is 1.5 V, with 1.6 V V_{CTRL} , the red signal is non-inverting gain signal of the VGA. With 1.4 V V_{CTRL} , the blue signal represents inverting gain signal of the VGA. With this approach, nine taps are easily controllable, and with different V_{REF} values, the gain range of the VGA improves too.

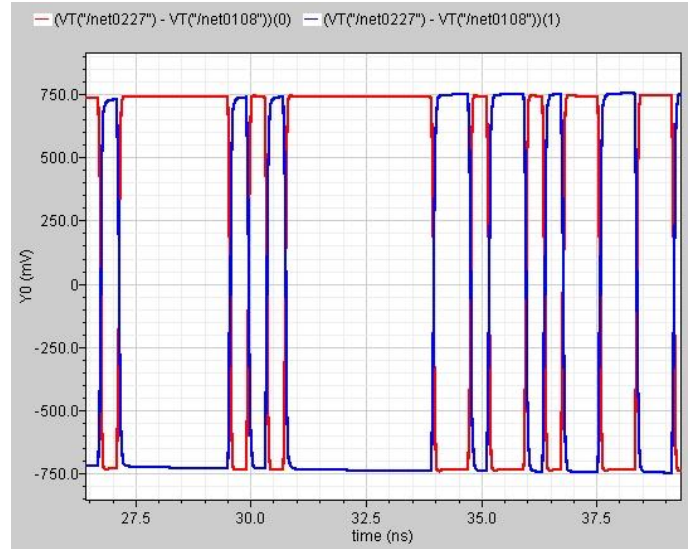
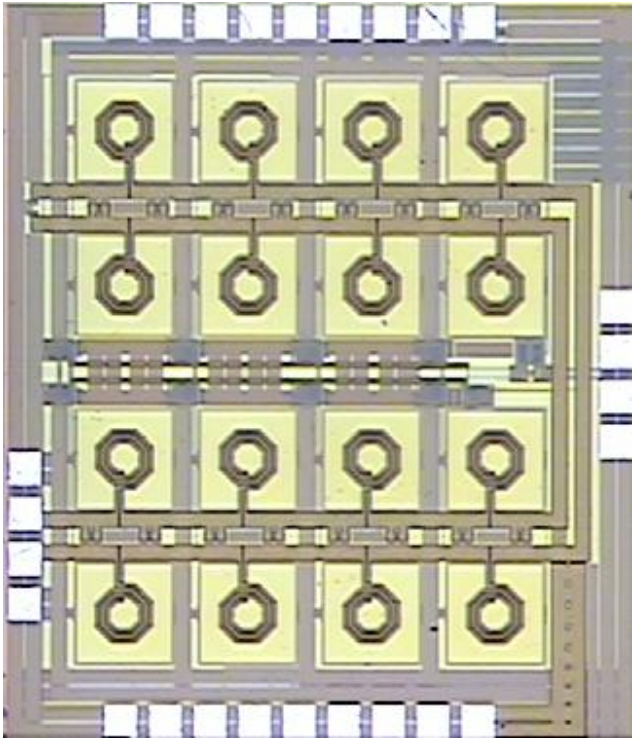


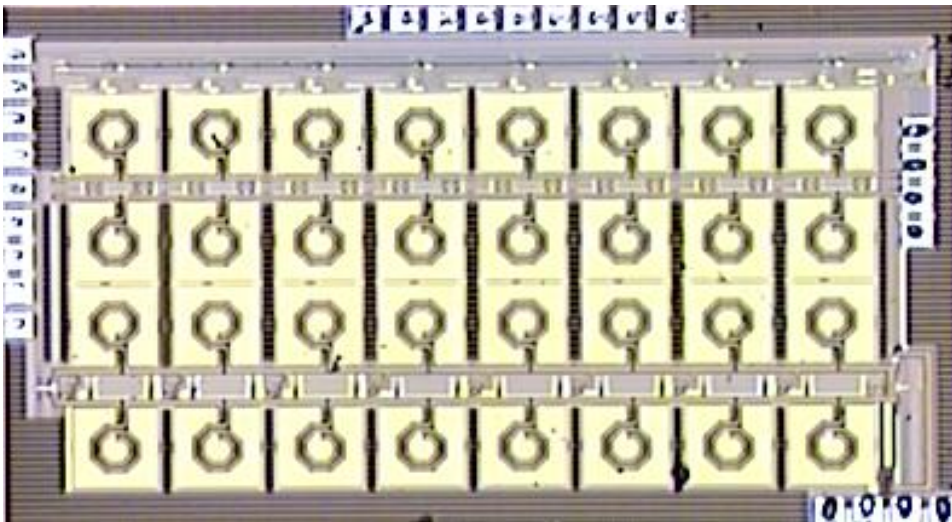
Figure 5-7. Simulation result of the balanced delay FFE VGA.

In addition to improving the bandwidth and voltage headroom, the balanced FFE offers reflection immunities as compared to its counterpart, the unbalanced FFE [62]. The impulse response from the FFE can be analyzed with reflection coefficients at the termination of the delay line. The first reflection from the unbalanced structure occurs at twice the frequency as that of the equalizer span and is proportional to the reflection coefficient at the termination. Because it is outside the FFE span, it can not be compensated for. The first reflection in the balanced structure is twice the strength of that of the unbalanced structure. However, since this first reflection is in the span of the FFE, it can be corrected by adapting the tap coefficients. The second reflection is too small to affect the equalizer transfer function for either of the FFE structures [63].

5-3. MEASUREMENT RESULTS OF EQUALIZERS



a) Unbalanced structure equalizer



b) Balanced structure equalizer

Figure 5-8. Microphotographs of the a) unbalanced and b) balanced FFEs.

Both structures are designed and fabricated in the 0.18 μ m TSMC CMOS process. Figure 5-4 shows microphotographs of the fabricated FFEs. Most of the area is occupied by inductors in L-C delay lines in both structures. The size of the unbalanced structure is 1.6 x 1.4 mm² and that of the balanced structure is 2.5 x 1.5 mm². The unbalanced structure has a smaller area compared to the balanced structure due to the fact that half the number of inductors used. Figure 5-5 shows a close match between the measured and simulated transfer characteristics of the balanced FFE for the 1st tap and the 9th tap. Figure 5-6 compares the measured transfer characteristic of the balanced and unbalanced FFE structures at the 1st and the 9th taps. At both of the taps, the balanced structure has a greater bandwidth than the unbalanced structure. The first tap has a bandwidth of 5.6 GHz in the balanced structure compared to a bandwidth of 3.5 GHz in the unbalanced structure. At the 9th tap, the balanced structure has a bandwidth of 2.3 GHz, while the unbalanced structure has a bandwidth of 0.8 GHz.

Measured S-parameter datasets are used to extract the group delay information. Figure 5-7 shows the extracted output at each tap of the balanced FFE for a step input with a rise time of 100 ps. A delay of 70 to 90 ps can be observed between the output responses of each adjacent tap. Table II lists the extracted tap delay for both of the FFE structures.

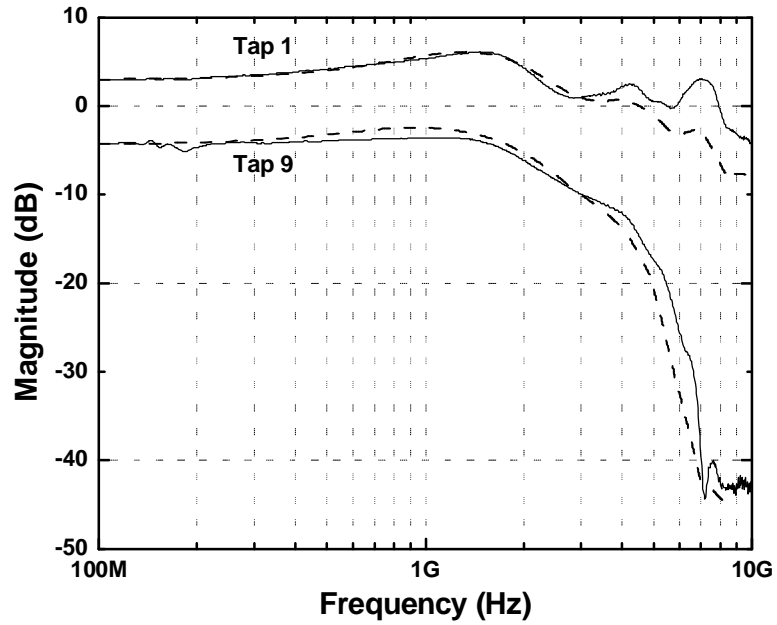


Figure 5-9. Simulated (dashed) and measured (solid) forward transfer characteristics of the balanced FFE structure.

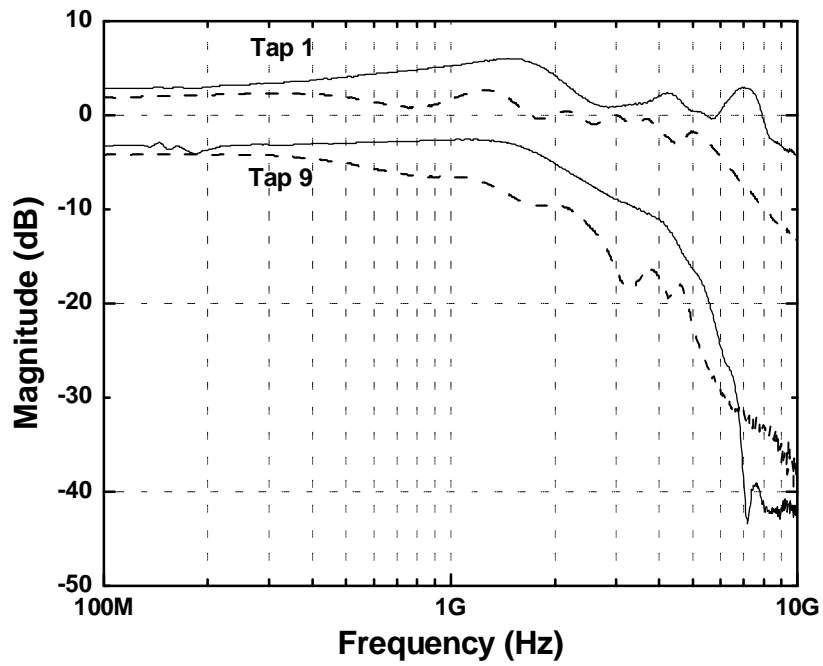


Figure 5-10. Comparison of the measured forward transmission gain of the balanced (solid) and unbalanced (dashed) FFE structures.

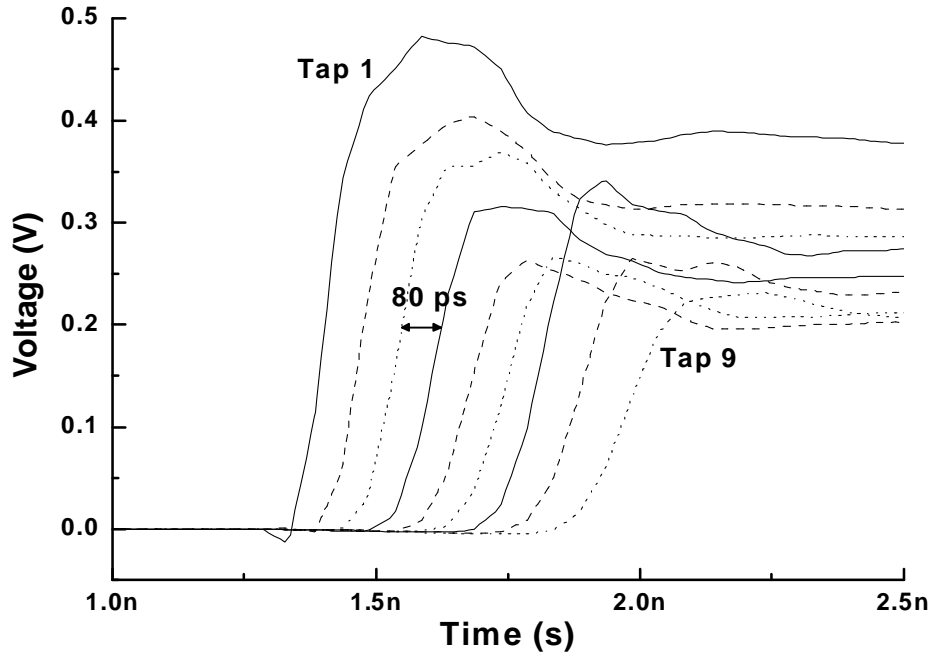


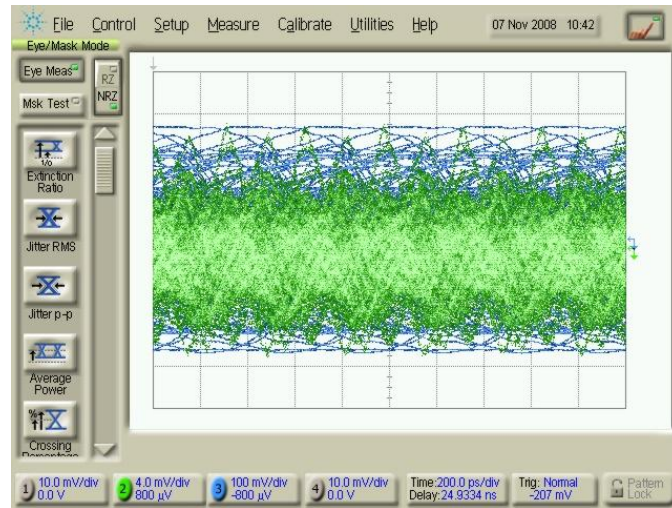
Figure 5-11. Extracted output response at each tap of the balanced structure for a step input.

TABLE II
EXTRACTED TAP DELAY

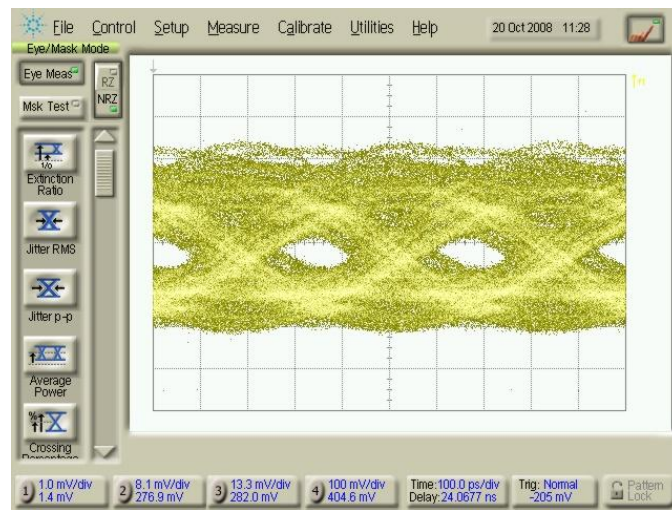
	Balanced FFE (ps)	Unbalanced FFE (ps)
Tap (1, 2)	70	72
Tap (2, 3)	72	84
Tap (3, 4)	72	47
Tap (4, 5)	78	74
Tap (5, 6)	66	74
Tap (6, 7)	56	76
Tap (7, 8)	88	70
Tap (8, 9)	101	78

Using two kinds of backplanes, 30 and 60 inch backplanes with 3 Gbps signal, experiments are conducted to verify the performance of the balanced FFE. In Figure 5-8, an eye diagram shows the opening in the middle for a 30 inch backplane. Also a 60 inch backplane with equalization shows the eye opening in Figure 5-9. In another view of equalization, the pulse signal feeds into the system to compare the signal before and

after equalization. Figure 5-10 and 5-11 show that the post-cursor ISI is cancelled after equalization because signal width has become sharper compared to the width of the initial signal.

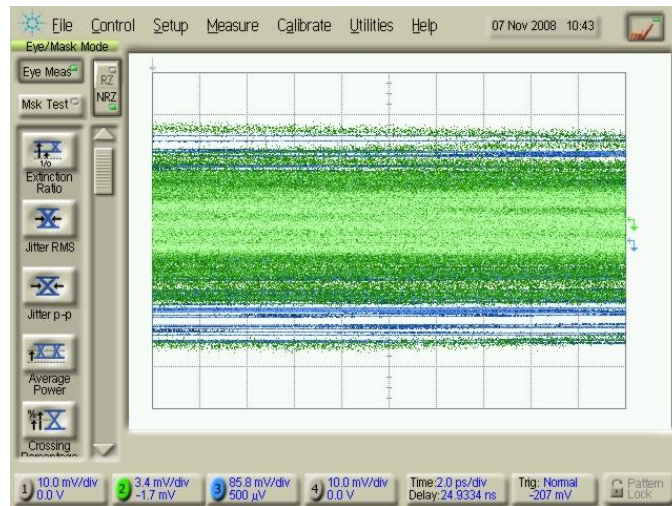


a)

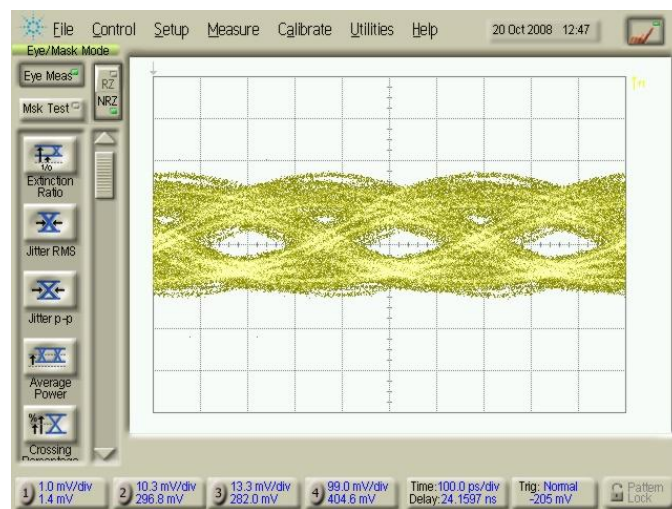


b)

Figure 5-12. Measured performance of the balanced FFE with a 3 Gbps NRZ data input of a 30 inch backplane a) before and b) after the equalization.

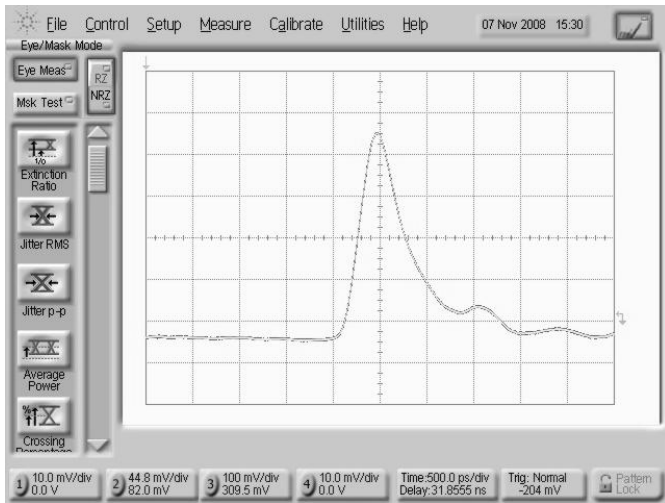


a)

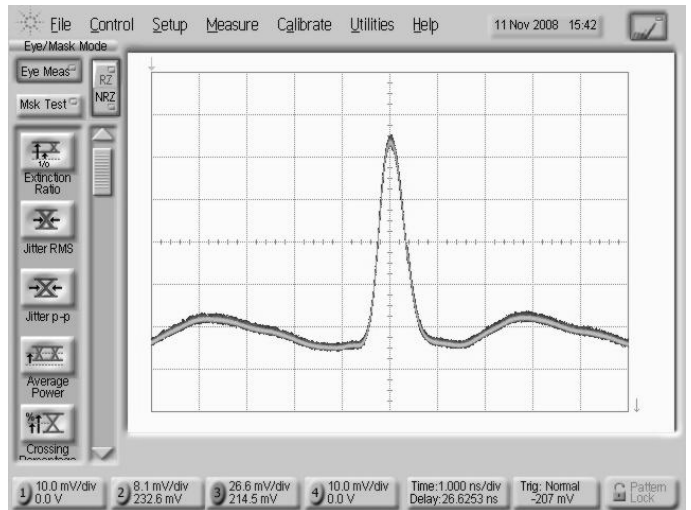


b)

Figure 5-13. Measured performance of the balanced FFE with a 3 Gbps NRZ data input of a 60 inch backplane a) before and b) after the equalization.



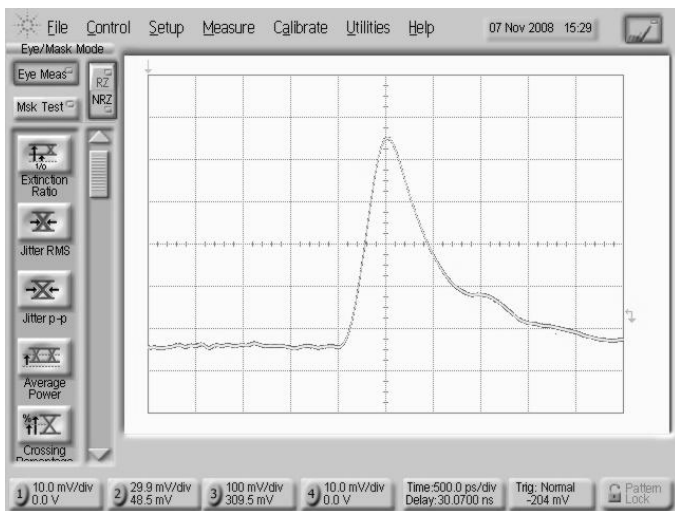
a)



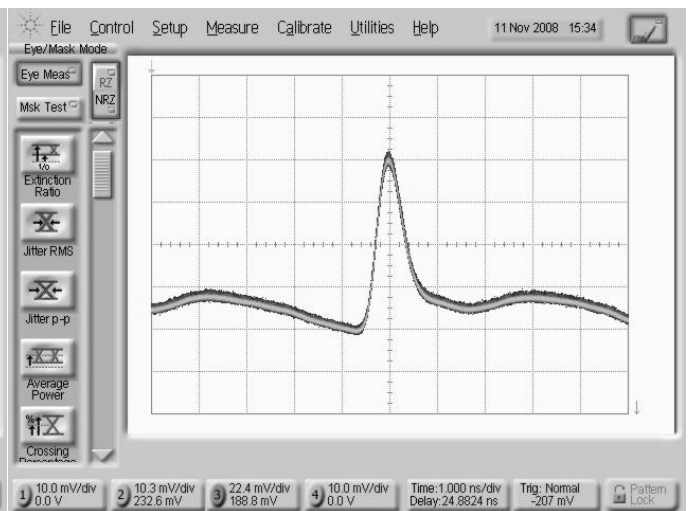
b)

Figure 5-14. Pulse measurement of unbalanced FFE with 33 ps width pulse input of a 30 inch backplane

a) before and b) after the equalization.



a)



b)

Figure 5-15. Pulse measurement of unbalanced FFE with 33 ps width pulse input of a 60 inch backplane

a) before and b) after the equalization.

This chapter has presented a comparative study of two different nine-tap passive delay line-based FFE structures. Both of the FFE structures are functionally equivalent, use the same building blocks, and are fabricated using 0.18 μm TSMC CMOS technology. The two FFEs differ only in the configuration of the delay paths and the relative placement of the cells. The balanced structure has greater bandwidth compared to that of the unbalanced structure and is less affected by the reflection at the delay line termination. Hence, it can be concluded that the structural configuration of the passive delay line based FFEs has a significant effect on the performance of the system.

CHAPTER VI.

ANALOG EYE OPENING MONITOR

6-1. SYSTEM SIMULATION OF EYE OPENING MONITOR

In previous chapters of this paper, it was mentioned that equalizers need to be adjusted with external voltage sources by a person monitoring an oscilloscope. However, if the equalizer tap weights can be adjusted automatically depending on different channel environments, the equalization system can be adaptable. To make the equalization system adaptable, it is necessary to verify the performance of the

equalizer [64, 65]. This can be achieved by measuring how clean the output signal of the equalizer has been in terms of signal integrity. The dispersion of the signal is mainly caused mainly by the high-frequency component loss through the band-limited channel. This causes ISI and closes the eye. Since the number of the high frequency components is proportional to the number of fast transitions, the performance of the equalizer can be measured by measuring the number of fast transitions.

The loss of high-frequency components makes the fast transitions of the signal, which occur at the edge of the square pulse, smoother and wider. In other words, the integrity of the received signal is improved as the high-frequency components of the transmitted signal experience less loss, letting more fast transitions of the signal occur.

The proposed eye-opening monitor (EOM) technique employs a simple architecture for lower power consumption while achieving the targeted data throughput. This output monitoring technique does not require clock and data recovery circuitry. This results in reduced complexity for easier circuit implementation. The analog EOM is placed at the output of the equalizer, as shown in Figure 6-1, to evaluate the overall signal quality. Instead of using clocked components, which can increase the complexity [66], the analog EOM employs two tunable delay cells and an integrator, as shown in Figure 6-2. The output signal from the equalizer is divided into two different delayed paths, where the delay amount of the first cell is set to capture the rise time and that of the second cell is adjusted to capture the fall time according to the data rate of the application. This tunable delay feature has the advantage of enabling the analog EOM to operate with applications with various data rates. The two delayed signals are then subtracted from each other, and the difference is subsequently integrated over time to generate a DC voltage. The eye opening size of the equalizer output signal will be directly proportional to the amplitude of the difference signal. Consequently, when this difference signal is integrated, the resultant DC value will also be proportional to the eye opening size.

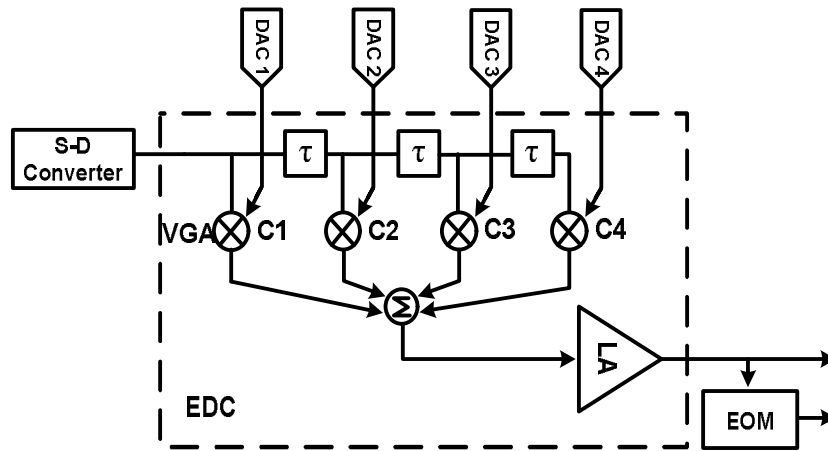


Figure 6-1. Analog EOM block with equalizer.

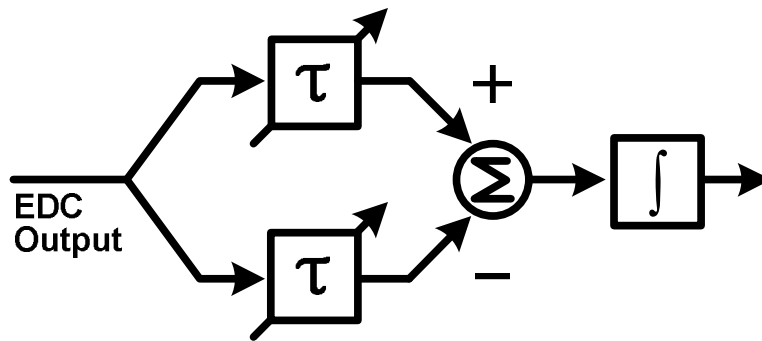


Figure 6-2. Analog EOM system block.

For example, a signal with a wide eye opening, as in Figure 6-3 (a) will have a larger integrated DC value than a signal with a narrow eye opening, as shown in Figure 6-3 (b). The signal quality of the equalizer, therefore, can be predicted without measuring the actual eye diagram. This information can be used to adapt the system.

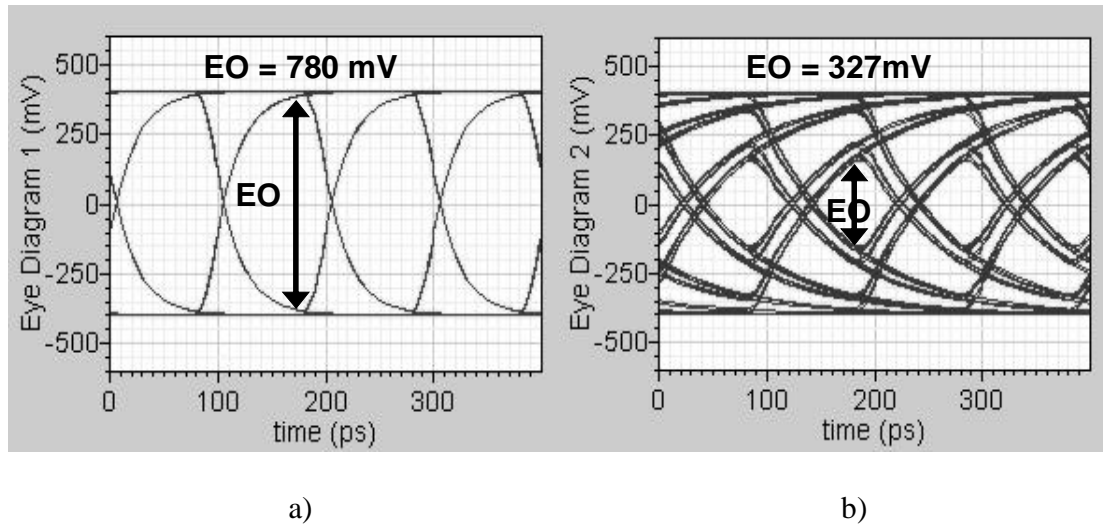


Figure 6-3. Different eye opening area.

6-2. COMPONENTS OF ANALOG EYE OPENING MONITOR

A tunable delay cell, as illustrated in Figure 6-4, consists of three active delay stages with a signal path that is connected to both the first and the third delay cells. The amount of signal distribution between these two delay paths is determined by the control voltage applied to V_{cont+} and V_{cont-} . These two delay paths form a slow path and a fast path. The fast path is designed to provide minimum gate delay, which can be achieved from the given process technology. The slow path, on the other hand, is designed to provide the longest desirable delay. The fastest path achieves a 15 ps delay, while the slowest path can achieve a delay of up to 95 ps. Figure 6-5 shows the simulation result of the tunable delay line. Figure 6-6 shows the relation between the control voltage and delay time.

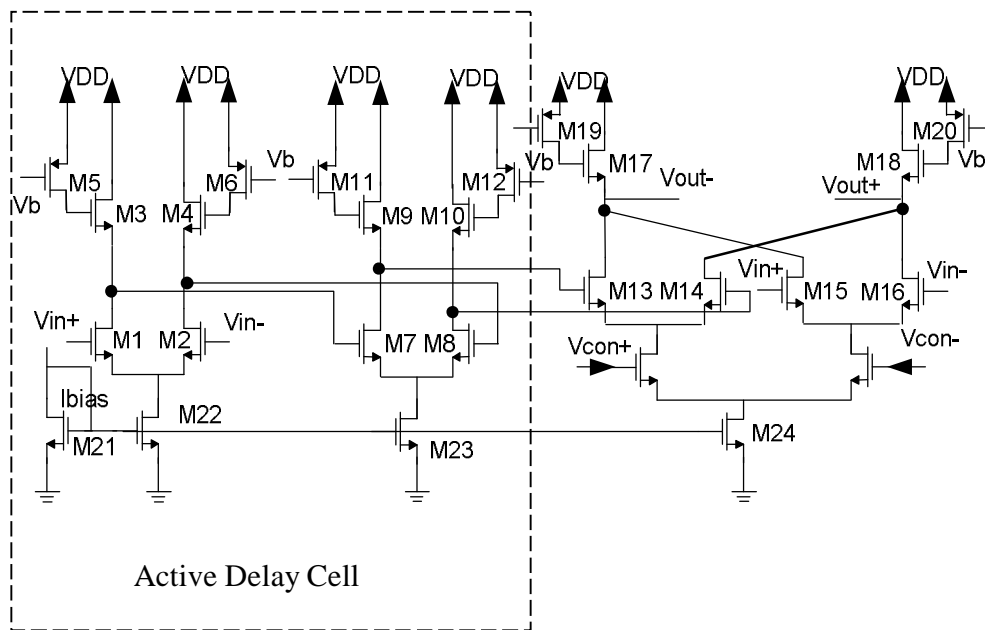


Figure 6-4. Schematic of tunable delay line.

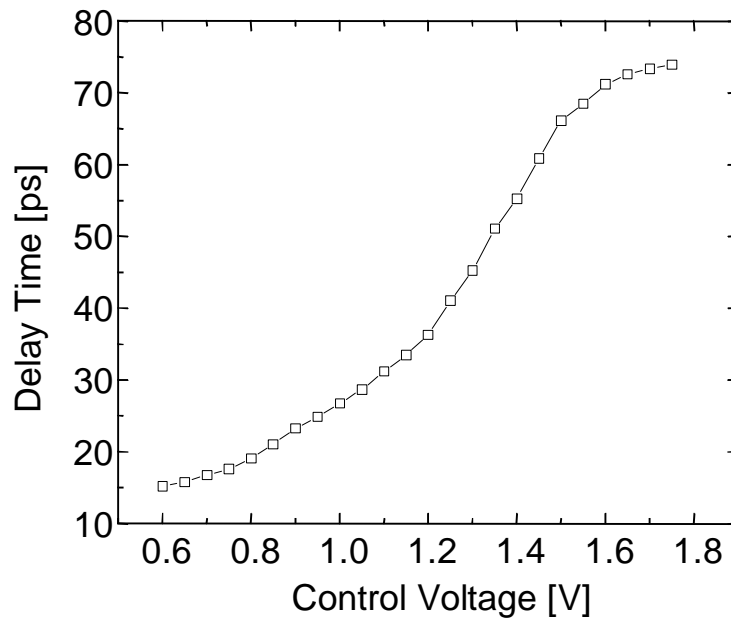


Figure 6-5. Delay time vs. control voltage.

A 6-bit digital-to-analog converter (DAC) is implemented to control the variable delay digitally. The schematic of the DAC is shown in Figure 6-7. A 6-bit DAC is integrated with each tap to provide control voltages. The R-2R ladder network architecture is used [67]. The design is modified to consist of bit-modules, as illustrated in Figure 6-7. This approach provides flexibility to the DAC resolution in that the desired number of bits can be designed by simply adding or deleting the standardized bit-modules [68]. This design is inherently accurate and easy to manufacture because an R-2R based modular DAC uses ratios of single value standardized poly resistors, where these ratios can be highly tolerant over process variation especially with an inter-digitated layout and added dummy resistors. To reduce error, which is critical for the equalizer, large aspect ratio devices are used for the NMOS switch transistors [69]. This feature minimizes errors due to voltage drop between the source and the drain.

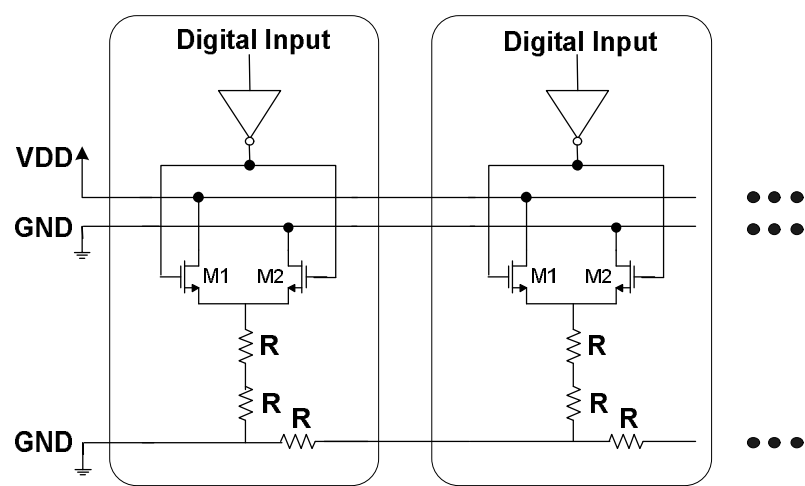


Figure 6-6. Schematic of the DAC.

Process corner simulations, supply voltage and temperature variations simulations are performed and showed ten percent of error offset at the least significant bit. The simulation result for the DAC is shown in Figure 6-8. Effective control range for the VGA is between 0.5 to 1.2 V, and corresponding gain is -1 to +1.

6-3. RESULTS OF ANALOG EYE OPENING MONITOR

The DAC and tunable delay line are fabricated on a single chip. The die photo is shown in Figure 6-9. The control voltage of the tunable delay line is connected to the DAC. Figure 6-10 shows the measurement results of the tunable delay line, illustrating linear control of the tunable delay for up to 82 ps, which closely matches the simulation results. A wide tuning range is achieved from 15 ps (fast delay path) up to 97 ps (slow delay path). This corresponds to the control voltage from 0.5 to 1.2 V, which is within the control range of the designed modular 6-bit DAC. These components are also fabricated in CMOS 0.18 μm process [70].

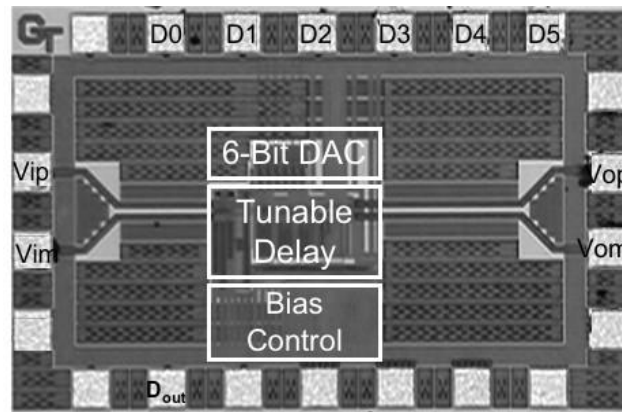


Figure 6-7. Die photograph of the tunable delay line with the DAC.

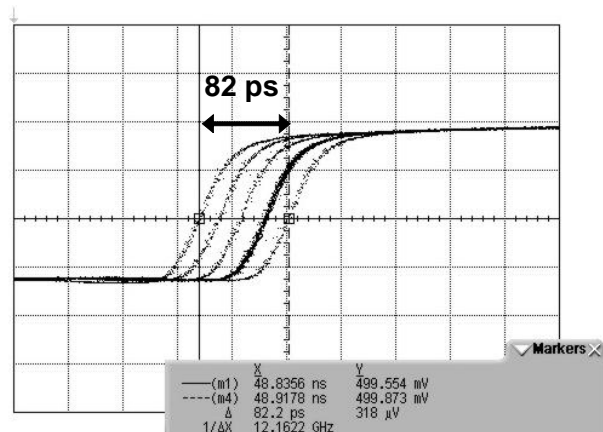


Figure 6-8. Measurement of tunable delay line.

The analog EOM is also fabricated with the CMOS 0.18 μm process, as shown in Figure 6-11. Finally, the results of the analog EOM are summarized in Table II. Three different eye diagrams with different eye-openings and their corresponding DC voltages show that, as expected, the bigger eye openings result in larger DC values from the analog EOM.

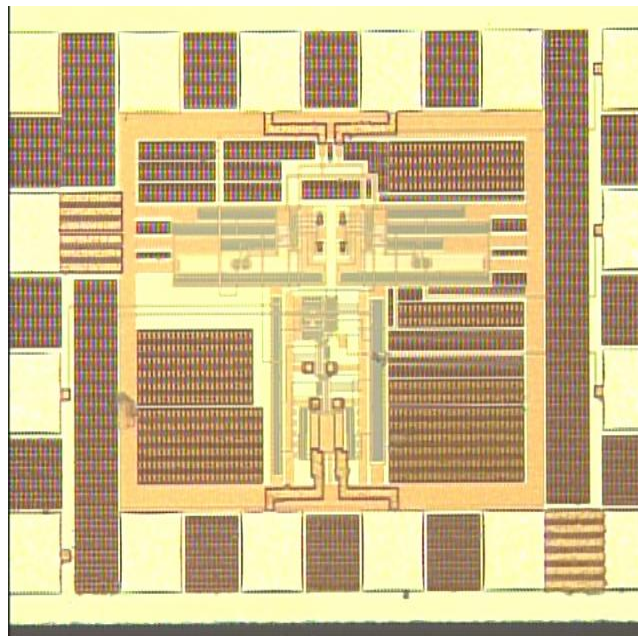


Figure 6-9. Die photograph of the analog EOM.

TABLE III
ANALOG EOM RESULTS

	Eye 1	Eye 2	Eye 3
EO	780 mV	527 mV	< 100 mV
Rise time	23.5 ps	90.4 ps	2.9 ns
Fall time	25.7ps	93.2ps	3.07ns
DC	713 mV	376 mV	187 mV

CHAPTER VII.

SUMMARY AND FUTURE RESEARCH DIRECTION

The object of this research is to develop the solution for band-limited channels. Backplane channel and GPON channel are investigated to apply the equalization technique. After the system simulation of the each channel, specification of the design is decided. The system simulation is based on the actual channel measurement to assure the accuracy of the simulation. Different lengths of backplane channels are measured with different signal speed to investigate the channel performance. Also the GPON system with different fiber lengths is implemented in the lab to measure the BER performance. Especially the GPON system utilizes the Fabry-Perot laser for the economic solution. After the implementation of circuits, circuits are inserted into the system to measure the performance of the channel with equalizers. Both cases show the successful channel improvement with measured eye diagram and the BER. Because it is controlled by

analog gains, measuring these channels requires time consuming procedure. To expedite the procedure and eventually build the adaptive system which could inserted and be optimized by itself, the monitoring the output of the equalizer is essential. The novel analog way to achieve this goal is suggested. Compared to its digital counterpart, it is compact and less power-consuming. All these equalizers mentioned here have one summing node to add up all the values from VGAs. This structure is very efficient in combining the signal but in case there are too many VGAs it draws too much current in the one node. This could be the problem for lowering voltage headroom and also bandwidth is limited because of large capacitance at one node. To mitigate these problem, the balanced equalizer architecture are suggested which uses the distributed amplifier method. With the same specifications, two nine tap equalizers are designed to compare the performance between the unbalanced structure and the balanced structure.

The original contribution of this research includes:

1. Investigated the BiCMOS and CMOS equalizer topologies for backplane channel equalization.
2. Investigated the GPON channel with Fabry-Perot noise and fiber dispersion
3. First to implement the EDC solution for the GPON system with Fabry-Perot laser.
4. Investigate the system requirement of the EDC for the GPON link with Fabry-Perot laser.
5. First to demonstrate the performance of the EDC with the actual GPON implementation with Fabry-Perot laser in the lab environment.
6. Designed the novel method to implement the eye-monitor scheme with tunable delay line.
7. Demonstrated the performance comparison between different equalizer structures with the same specification.

The dissertation begins with the introduction stating the communication channel is outgrown its usage because of the rapid increased use of the internet and other multimedia. To overcome this problem, various kinds of communication channels are utilized together to maximize its performance. One of the proposed solutions uses the short distance communication with the backplane channel and the long distance communication with the optical channel. Especially the GPON system is efficient way of communication because it can transmit various data together to end users with up-to 32 channels. These two channels have been used for sometime but the rapid increase of data traffic reaches the limit of both channels. In chapter 2, backplane channel and GPON channel are investigated for channel impairments respectively. Both channels have different sources of the channel impairment but it shows the similar outcome. Backplane channel has various noise sources such as skin effect and dielectric loss and they all contribute to ISI. This phenomenon gets worse with the increased distance and the speed. Eye diagrams and bath tub curves are shown to confirm the channel impairment. For the GPON channel, major sources of channel impairment are dispersion from the fiber and noise from the Fabry-Perot laser. Dispersion from fiber is also increased with the longer fiber length. These noise sources in the GPON link impeded the data transmission of the channel. To improve the bandwidth and the BER, the equalization technique using silicon device provides the one chip solution cost effectively for both channels. The concept of the equalization technique is explained using the time and frequency domain. Also various equalization techniques are explained, too.

In chapter 3, equalizer circuits for backplanes are designed using CMOS 0.18 μm and BiCMOS 0.25 μm process. 10 Gbps data transmission is targeted for the backplane communication. As demonstrated previously with the eye diagram, 20 inch backplane can not recover the data over 5 Gbps. Based on S-parameter measurements system simulations are performed to decide the equalizer's specifications. Two types of the equalizer are suggested with different implementation of the delay line. Passive L-C delay line is the ladder structure with stable delay over the frequency but inductors occupies too much of physical

space. Another approach is using propagation delay of active devices. To improve the bandwidth of the equalizer, inductive peaking technique using active devices are implemented. Doing so, the physical area efficiently is optimized compactly with no use of inductors. For CMOS case, the voltage headroom is limited but using folded cascoded device makes implementation possible with enough gain for equalization. BiCMOS solution has advantages in the voltage headroom and bandwidth than CMOS process. BiCMOS and CMOS fabrication is sponsored by National Semiconductor Inc. Experimental results for both equalizers show successful the channel improvement with actual backplanes. Experimental results are shown in eye diagrams comparing the backplane channel with the equalizer and without the equalizer.

In chapter 4, the components of the GPON system is investigated. Because Fabry-perot laser and the fiber is the major source of the channel impairment, these two factors are modeled with mathematical terms. These models are tested comparing simulations with actual measurement of the GPON channel. Two BER graphs shows close match to confirm the accuracy of the models. Using these models, power penalty from noise sources are also simulated. Based on these simulations, the system simulations of the channel with the EDC are performed and the specification of the circuit is decided. The EDC for the GPON link is designed with the active delay line for the minimized area. Because of its large delay amount (267 ps), using passive device means unrealistic huge inductors. Actual circuit is designed using TSMC CMOS 0.18 um process sponsored by the Pirelli Broadband Solution Inc. With Pirelli's Fabry-Perot laser and other optical components, the GPON system is implemented in the laboratory. To include the EDC in the system, optical signal needs to be converted to electrical signal. Bit pattern and BER data are measured for both with the EDC and without the EDC cases. Bit pattern shows the clean signal with the EDC and BER data shows about 3 dB improvements in the received optical power at the same BER with two different wavelengths.

In chapter 5, structural differences of equalizers are investigated. Previous approaches in this research all have one delay element in the input side of the signal path. Using distributed amplifier structure,

delay elements are divided into two and placed evenly at the input and output side. Because of that, it is suggested to be called the balanced delay structure. Two nine-tap equalizers are designed using this balanced delay approach and unbalanced delay approach with the same specification. Comparison shows the improved bandwidth and gain of the balanced delay structure over the unbalanced delay structure. Using this new balanced structure 20 inch backplane is successfully equalized showing the open eye diagram at 10 Gbps.

Last chapter covers the control of tap gains of the equalizer. Different channel needs different settings of the tap gains of the equalizer. Because it changes over different channels, some type of output monitoring scheme is needed to evaluate the equalizer performance. Using the fall time and rise time difference of the signal, signal integrity can be captured. This system requires only the simple subtraction block and tunable delay line for different signal speed. The output of this eye monitor shows the different DC values according to the signal integrity.

As a future research, other applications such as the wireless handset could be beneficial from this research. Because nowadays the wireless handset handles many different data in the small unit, there are interferences between signal. This will make the overall signal quality degraded. Using the technique like equalization, signal interference in the handset can be reduced. Another approach to improve the system would be realizing the adaptive system. Using eye monitoring scheme as stated in this dissertation, DC values according to signal quality can be used to change the tap gains of the equalizer. Using algorithms like LMS, optimum solution could be provided and it could be updated with changing channel conditions. This will enable the equalization system fully adaptive and could be covered wider channel conditions.

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VITA

Hyoung Soo, Kim received the B.S. degree from Yonsei University, Seoul, Korea in 1999 and the M.S. degree in Electrical and Computer Engineering from Georgia Institute of Technology, Atlanta, GA in 2004. From 2004, he has been with Microwave Application Group (MAG) as a Ph.D. student. He also worked as a Co-op student for Lyric Semiconductor; a DARPA funded startup-company from Massachusetts Institute of Technology (MIT), twice in 2008 and 2009. His works as a Co-op student include various analog and digital circuit designs. Currently, he is a full-time Ph.D. student at Georgia Institute of Technology. His research interests include mixed-signal circuit and system designs with focus on the signal integrity improvement with noise cancellation, and equalization techniques for 10+Gb/sec broadband communication applications.

